Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

III SEMESTER B.TECH. (INFORMATION TECHNOLOGY)

END SEMESTER EXAMINATIONS, NOVEMBER 2018

SUBJECT: DIGITAL SYSTEMS [ICT 2102]

REVISED CREDIT SYSTEM
(22 /11 /2018)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data if any, may be suitably assumed.

1A. Simplify the given function 'F' using tabulation method. Implement the simplified expression using basic logic gates. **5**

$$F(A,B,C,D,E) = \sum m(2,11,13,14,15,24,27,29,30) + \sum d(0,12,16,18,25,28,31)$$

1B. Using PROM of smallest appropriate size, draw the logic diagram in PLD notation to realize the arithmetic expression F(X) = 3X +2 for $0 \leq X \leq 7$, where F(X) and X are binary numbers. **3**

1C. Design a sequential circuit to generate the sequence 1011 using ring counter and external gates. **2**

2A. Design a code converter to convert a decimal digit represented in 8 4 -2 -1 to a decimal digit represented in gray code using NOR gates ONLY. **5**

2B. Design JK flip flop using NOR latch and external gates **3**

2C. Construct 4:2 priority encoder using basic logic gates. **2**

3A. Design a 4 – bit × 4 – bit binary multiplier using full adders and external AND gates ONLY. **5**

3B. Design an asynchronous presettable counter to count from $3_{(16)}$ to $B_{(16)}$ using D flip flops and external gates. **3**

3C. Using 7490 ICs ONLY, design a counter to count from 00 to 87 continuously. **2**

4A. Design a sequential logic circuit to count in decimal from N2 to N1 where N2 >N1 using 7483 ICs, 74193 ICs, 74157 ICs and external gates. N1 and N2 are two 8- bit numbers. **5**

4B. Design a logic circuit to perform arithmetic operation F=XY when M=0 and perform F=X+Y when M=1 using minimum 74153 ICs ONLY. Assume X and Y are 1 – bit binary numbers and F is a 2-bit binary number. **3**

4C. Simplify the given function 'F' using K- Map into product of sums form. $F(A,B,C,D,E) = \sum m(1,3,5,7,9,11,13,15,25,27) + \sum d(2,8,21,23,28)$ **2**

5A. Design a Moore sequence detector circuit to detect the sequence 110 and 01101 using T- flip flops and external gates. Overlapping of the sequence is allowed. **5**

5B. Design 1-bit magnitude comparator with cascading inputs using logic gates. Using the same, draw the circuit to compare two 4-bit binary numbers. **3**

5C. Design 4 to 16 line decoder using 2 to 4 line decoders only. **2**