Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

III SEMESTER B.TECH. (INFORMATION TECHNOLOGY)

MAKE UP EXAMINATIONS, DECEMBER 2018

SUBJECT: DIGITAL SYSTEMS [ICT 2102]

REVISED CREDIT SYSTEM
(24 /12 /2018)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer ALL the questions.
- Missing data, if any, may be suitably assumed.

1A. Design a code converter to convert a decimal digit represented in 8 4 -2 -1 to a decimal digit represented in Excess - 3 code using NAND gates only. **5**

1B. What is a race around condition? How is it overcome using Master-Slave configuration? **3**

1C. Draw the sequential circuit for MOD – 6 Johnson counter and show that each state can be decoded using 2 – input AND gates ONLY. **2**

2A. Simplify the Boolean function $F(A,B,C,D) = \prod M(0,1,6,7,9,14,15) \bullet \prod \phi(5,13)$ using Quine McCluskey method and draw the logic circuit using NOR gates ONLY. **5**

2B. An asynchronous circuit divides an input square wave by a factor of 14 and produces an output waveform with 50% duty cycle. Give the circuit realization using negative edge triggered JK flip flops and external gates. **3**

2C. Using Mealy model, write the state diagram for detecting the binary sequence 1101 in the input binary steam. Overlapping of sequence is allowed. **2**

3A. Design a 4-bit binary Carry Look Ahead adder circuit. Discuss its merits over a 4-bit binary ripple carry adder. **5**

3B. Design SR flip flop using NAND latch and external gates. **3**

3C. Design a 2-digit decimal down counter using 74193 ICs and external gates. **2**

4A. Design a synchronous counter to count the sequence 0 → 1→ 4 → 6 → 0 when external control input X is LOW and 6 → 4 → 1 → 0 → 6 when control input X is HIGH. Use T – flip flops for the design with minimal external gates. Undefined states should lead to state 6 during the next clock. 5

4B. Design a 4 – bit magnitude comparator using 7483 IC and external NOR gates only. 3

4C. Design a full adder using 74138 IC and minimum external gates. 2

5A. With the help of neat diagrams, explain three different types of programmable logic devices. Also, implement the following logic functions using suitable PLA. $f_1 = \sum m(0,3,4,7) and \quad f_2 = \prod M(2,4,5)$ 5

5B. Design a 2 – bit × 2 – bit binary multiplier using 74151 ICs and external gates. 3

5C. Draw the logic circuit of 2-bit presettable asynchronous counter using D flip flops and external logic gates. 2