Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

THIRD SEMESTER B. TECH. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER DEGREE EXAMINATIONS, DECEMBER – 2018

SUBJECT: DIGITAL ELECTRONIC CIRCUITS [ICE 2103]

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A Minimize the following function using K-map. 3M

$F(X_1, X_2, X_3, X_4) = \Sigma\, m(1, 3, 5, 7, 8, 9, 12, 13) + d(14, 15)$

1B Design a combinational circuit that accepts a 3-bit BCD number and generates an output binary number equal to the square of the input number. 4M

1C Implement the following Boolean function using 8:1 multiplexer. 3M

$F(A, B, C, D) = A\bar{B} + BD + \bar{B}C\bar{D}$

2A The input signals shown in Fig. Q2A are applied to an S-R flip flop with active - HIGH PRESET and CLEAR. Draw the output waveform for (i) a positive and (ii) a negative edge triggered S-R FF. Include the clock waveform in the solution. Present state of the flip flop, Q = 0. 3M

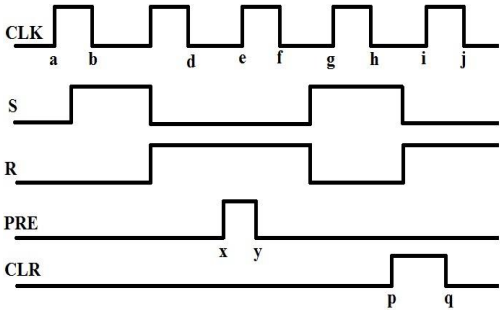

Fig. Q2A

2B Differentiate between combinational and sequential circuits. 2M

2C Explain in detail all the flip flop operating characteristics with relevant figures. 5M

3A Design a Mod – 7 asynchronous counter using JK Flip flops. 4M

3B Explain the working of a Ring Counter with neat logic diagram, timing diagram and the count table. 3M

3C Draw the ASM chart for a Mod 6 Counter. 3M

4A Explain parallel shift registers with neat diagrams. 5M

4B Draw the state diagram for a Moore type sequence detector to detect the sequence 110. Implement the sequence using D flip flops. 5M

5A Explain Hazards in sequential circuits. 4M

5B Explain in detail the architecture of PLA. 3M

5C Show how the PROM circuit would be programmed to implement the sum and carry outputs of a full adder. 3M

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