III SEMESTER B.TECH. (MECHATRONICS ENGINEERING)

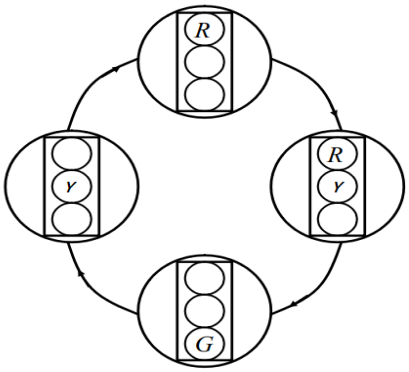
END SEMESTER EXAMINATIONS, NOV 2018

SUBJECT: DIGITAL INTEGRATED CIRCUITS AND APPLICATIONS [MTE 2105]

(29/11/2018)

Time: 3 Hours MAX. MARKS: 50

1A	Describe the race around condition in JK flip flop. Also mention the methods used to overcome it.	**02**
1B	Realize a 3 bit odd parity generator using CMOS.	**03**
1C	Design a circuit to detect a sequence of 101 with overlapping allowed. Implement using D flip flop.	**05**
2A	Implement a full subtractor circuit using 4X1 Multiplexer.	**03**
2B	Design a combinational circuit using IC 74LS83 and logic gates for the following application. Ajay and Vinay went to buy notebooks in the shop. Ajay bought "X" number of notebooks and Vinay bought "Y" number of notebooks. If total notebooks bought by them are more than or equal to one dozen then the shopkeeper will give 5 pieces free. Design the circuit using Full Adder IC to find out how many pieces Ajay and Vinay get altogether.	**03**
2C	Implement a combinational circuit for a control panel's light using i) Logic gates for K map minimized equation. ii) Using active high Decoder. The panel light in a control room at the launching of a satellite is to go "ON", if the pressure in both fuel and oxidizer tanks is equal to or above the required minimum and there are less than 10 minutes for lift off. Or, if the pressure in the oxidizer tank is equal to or above a required minimum and the pressure in fuel tank is below but there are more than 10 minutes lift off. Or if the pressure in oxidizer tank is below the required minimum but there are more than 10 min to lift off.	**04**
3A	Convert SR flip flop to JK flip flop.	**03**
3B	Draw the stick diagram of AND, OR and EXOR gates using P channel MOSFET.	**03**

3C	Generate a circuit for a counter, which is to be used in a food processing industry, where a machine performs the task of packing 6 gems per packet. A digital up counter, synchronised with a same clock pulse is used to perform the task. Also predict the behaviour of the counter circuit if an invalid state of the machine is encountered in the counting sequence.	**04**
4A	Design a serial adder circuit using Mealy model.	**05**
4B	Draw state diagram for NOR latch.	**02**
4C	Generate a pulse train signal circuit that blinks LED for home lightening system, in which the LED is ON for a duration of 3 sec and OFF for 1 sec. There after the process is repeated. The operating frequency of the circuit is 1 Hz.	**03**
5A	Determine the decimal and base 5 value, of the digit 100011010001 written in a new Binary Coded number system in which every digit of base 5 is represented by its corresponding 3 bit binary code. For example number 24 in base 5 is written as 010100	**02**
5B	Design a circuit to repeat the following sequence using synchronous sequential circuits of D flip flop. Where, R, Y and G represent the Red, Yellow and Green lights of a traffic control signal system. The operating sequence for the same is given as shown in Fig.1B.  Fig.5 B.	**03**
5C	Draw the state diagram and design a sequential circuit for error detector using D Flip Flop and Mealy machine for the following application. A digital circuit receives a bit stream of 1's and 0's randomly as input and it should produce the output same as input till it encounters two number of consecutive bits as 0's. After it must produce bitwise complement of the input until it encounters two consecutive bits as 1's.Then the process repeats.	**05**