MANIPAL ACADEMY of HIGHER EDUCATION
(Deemed to be University under Section 3 of the UGC Act, 1956)

Reg. No.										

DEPARTMENT OF SCIENCES, I/III SEMESTER M.Sc. (PHYSICS)
END SEMESTER EXAMINATIONS, December 2018 – Make up
SUBJECT : Fundamentals of Electronics [PHY 4107]
(REVISED CREDIT SYSTEM-2017)

Time: 3 Hours MAX. MARKS: 50

Note: (i) Answer **ALL** questions

(ii) *Draw diagrams, and write equations wherever necessary*

1. (a) Sketch the logic system for a clocked SR and JK flip flop and give their truth tables. (3M)
(b) Use a Karnaugh map to minimize the following standard SOP expression
$\bar{W}\bar{X}\bar{Y}\bar{Z} + W\bar{X}YZ + W\bar{X}\bar{Y}Z + \bar{W}YZ + W\bar{X}\bar{Y}\bar{Z}$ (4M)
(c) Define a demultiplexer. Draw the logic diagram for a four input multiplexer. (3M)

2. (a) Describe the operation of two-bit simultaneous A/D converter with suitable logic diagram and give the logic expressions for the 2^0 and 2^1 bits. (5M)
(b) Draw the four-bit binary ladder. Find the expressions for the voltages due to MSB and LSB. (5M)

3. (a) Draw the circuit diagram for differential amplifier and obtain an expression for voltage gain for single ended operation. (4M)
(b) Explain how op-amp can be used as a first order high pass filter and obtain an expression for its lower cut off frequency. (4M)
(c) The intrinsic stand off ratio for a UJT is 0.6.If the inter-base resistance is 10KΩ, what are the values of R_{B1} and R_{B2}. (2M)

4. (a) Drawing the block diagram of timer 555 explain how it can be used for monstable operation. Draw the waveforms at the threshold and output terminals for a given trigger input. (5M)
(b) Show how op-amp can be used as a Schmitt triger and explain its operation. (3M)
(c) Discuss the operation of an op amp as an inverting amplifier. (2M)

5. (a) Draw the voltage divider bias circuit diagram for a n type bipolar transistor in common emitter configuration.Using Thevenin's equivalent network obtain an expression for the base current. (4M)
(b) Define quality factor .Obtain an expression for quality factor for a series RLC circuit and arrive at a relationship between quality factor and band width. (4M)
(c) What are the advantages of FET over BJT. (2M)