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# MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

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**FIRST SEMESTER M.TECH. (DEC&MICRO) DEGREE END SEMESTER EXAMINATION**
**DECEMBER 2018/JANUARY 2019**
**SUBJECT: ANALOG AND RF VLSI DESIGN (ECE - 5102)**

**TIME: 3 HOURS** **MAX. MARKS: 50**

**Instructions to candidates**
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Discuss the frequency response of common source amplifier by considering high-frequency small signal analysis.

1B. Find the expression for resistance **Z** for the circuits shown in **Figure 1B**.

1C. Show that a negative capacitance can be realized using an amplifier block having variable gain A and a passive capacitor C. State the principle used.

(5+3+2)

2A. i. Bring out the differences between Op-amp and OTA.
ii. With a schematic circuit explain the working of an unbalanced CMOS OTA. Give the expression for dominant and non-dominant pole frequency. Bring out the differences between unbalanced and balanced OTA.

2B. Design a double cascode current mirror to sink a current of 10 μA. Find the minimum voltage across the current sink and the output resistance. Given that $K_n$ = 50 μA /$V^2$, $V_{gs}$ = 1.2 V, $V_{thn}$ = 0.83 V, $V_{thp}$ = 0.91 V, λ = 0.06 $V^{-1}$, $V_{DD}$ = 2.5 V, $V_{SS}$ = -2.5 V.

2C. Discuss improved wide-swing cascode current mirror circuit(s).

(5+3+2)

3A. Derive the expression for the small-signal voltage gain $A_v$ for NMOS ($M_1$) CS stage with diode-connected PMOS load ($M_2$). Given that $(W/L)_1$ = 100/1, $(W/L)_2$ = 20/1, $K_n$ = 2.5 $K_p$ and $I_{ds1}$ = $I_{ds2}$ = 0.5 mA. Assume λ = 0. Calculate the small-signal voltage gain $A_v$.

3B. **i.** Obtain the expression for small-signal voltage gain for the circuit shown in **Figure 3B** neglecting second-order effects.
ii. Explain the channel length modulation. Give the expression for channel length modulation parameter (λ).

3C. Derive the expression for small-signal common-mode voltage gain in a source-coupled NMOS differential amplifier neglecting second-order effects.

(5+3+2)

4A. Define and explain the significance of following parameters with respect to MOS device:
i. γ ii. η iii. $L_{electrical}$ iv. $L_{effective}$ v. λ

4B. i. Show how PLL can be used for FM demodulation.
ii. Explain common centroid geometry layout technique.

4C. Define the term single parameter sensitivity. Derive an expression for sensitivity of output current $I_o$ with respect to $V_{DD}$ in a cascode current sink circuit. Give your comments.

(5+3+2)

5A. Consider a NMOS CG amplifier with a passive resistive load $R_D$. Derive the expression for following: (i) small-signal voltage gain (ii) input impedance (iii) output impedance with and without channel length effect. Give your comments.

5B. i. Explain the concept of half-circuit as applied to differential amplifiers with an example.

ii. With appropriate figure, explain how the differential operation can reduce effect of supply noise.

5C. Explain how the differential operation can reduce following: [i] effect of supply noise [ii] Effect of coupled noise from digital clock signal.

(5+3+2)

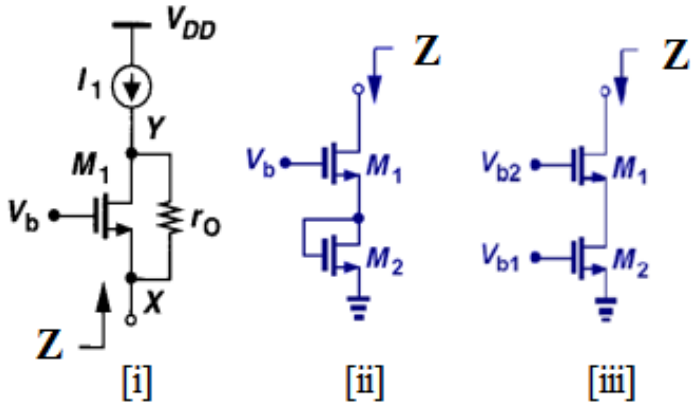


**Figure 1B**

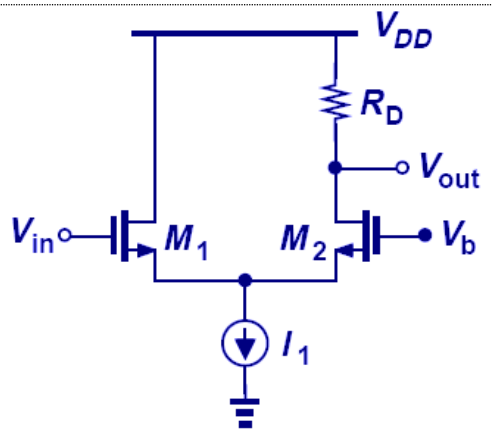


**Figure. 3B**