Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

FIRST SEMESTER M.TECH. (ME) DEGREE END SEMESTER EXAMINATION
DECEMBER 2018/JANUARY 2019
SUBJECT: ADVANCED DIGITAL VLSI DESIGN (ECE - 5121)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Estimate the raise time and fall time of a CMOS inverter and establish the condition for obtaining symmetrical operation.

1B. Compute the rise time and fall times in terms of *'τ'* for a CMOS three input NAND gate designed with feature sized transistors. If we need to make the rise time and fall times equal for worst case condition, calculate the device sizes.

1C. With respect to interconnects in VLSI discuss the following issues:
i) Inductive parasitics and ii) Cross talk

(4+3+3)

2A. Implement F=((A+B)C)' using CMOS gate logic. Draw the lay out using Euler path method and estimate the minimum area required.

2B. With the help of neat diagrams, explain the fabrication of CMOS inverter using SOI process. What are its merits and demerits?

(5+5)

3A. With the help of a circuit diagram explain BiCOMS logic. What are the merits and demerits of the logic? Briefly explain.

3B. List the objectives to be met while developing clock distribution and describe with the help of neat sketches the clock distribution strategies employed in VLSI with their salient features.

3C. With the help of suitable diagrams, discuss clock skew and jitter along with their impact on the circuit performance.

(4+3+3)

4A. What is meant by general scaling? Explain. Also illustrate the impact of general scaling on the following parameters: i) Gate Capacitance ii) Current density and iii) Maximum operating frequency assuming that supply voltage and oxide thickness are scaled by $1/\beta$ while, all other parameters are scaled by $1/\alpha$.

4B. With the help of neat diagrams explain clock distribution techniques. Also discuss their salient features.

4C. Draw the circuit of a functionally complete static SR flip flop and list its salient features.

(5+3+2)

5A. With the help of a neat circuit diagram explain the read and write operation in a 3-T DRAM cell. Also highlight its salient features.

5B. Show the complete architecture of 4 MB SRAM memory assuming that the architecture has 16 blocks/banks and each block is square in shape.

(5+5)