Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FIRST SEMESTER M.TECH. (DEC & ME) DEGREE END SEMESTER EXAMINATION
DECEMBER 2018/JANUARY 2019
SUBJECT: PROCESSOR ARCHITECTURE & APPLICATIONS (ECE – 5103)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Describe architectural overview, memory system of TMS320C64x digital signal processor.

1B. Discuss all types of addressing modes with examples of Digital Signal Processors.

1C. Explain Interrupt I/O strategy with algorithm / program used for implementation.

(4+3+3)

2A. Write programming model/architecture of Mixed Signal Microcontroller and its application.

2B. Discuss centralized and distributed memory architectures in multiprocessors.

2C. Interface processor to 2K byte RAM using address decoder and other logic circuits. Assume starting address 0000F800H.

(4+3+3)

3A. With a diagram, show the complete multi cycle data path implementation scheme for implementation of instructions.

3B. How valid translations in page tables happen in ARM MMU. Explain all methods with necessary diagrams.

3C. Describe cache optimization techniques to reduce miss rate.

(4+3+3)

4A. Discuss compiler based solution to enforce coherence in a centralized shared memory architecture. Two processors A and B are connected to a enforce memory. Initial content of memory location M is FFH. CPU A reads the content of memory location M and then writes 00 to M. With the help of different protocols, narrate the bus activities and updating of contents in caches of different processors.

4B. If sum of 256 products are to be computed using MAC, with execution time 100 n sec, compute total time to complete the operation. Modify the MAC unit to prevent overflow condition. A 8 tap FIR filter with maximum sampling time = 1/4T. Show the implementation of the filter with necessary diagram.

4C. With necessary diagram, explain architectural features of memory vector Processor.

(4+3+3)

5A. A superscalar pipelined machine, capable of fetching and decoding two instructions at a time, having three functional units (F1 & F2 are 2 integer functional units + F3 is a 1 floating point). Each instruction takes one cycle to execute. Two instances of write back stages.

Given: Ten instruction code segment (I1 to I6)

- I1 requires two cycles to execute
- I3 and I4 conflict for functional unit F3
- I5 depend on value produced by I4
- I5 and I6 conflict for functional unit F2

Implement the above code using **two policies** which take maximum number of clock cycles.

5B. Describe register renaming in ILP , with examples.

5C. With necessary diagram, analyse pipelining adopted in Pentium 4

(4+3+3)