Question Paper

Exam Date & Time: 24-Nov-2018 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

SCHOOL OF INFORMATION SCIENCES

FIRST SEMESTER MASTER OF ENGINEERING - ME (EMBEDDED SYSTEMS)

Advanced Computer Architecture [ESD 611]

Marks: 100 **Duration: 180 mins.**

END SEMESTER DEGREE EXAMINATION NOVEMBER 2018

Answer all the questions.

1) A. List out the difference between combinational and sequential Logic Circuits B. Define the following with suitable examples: (5 * 2) (10)
Minterms
Maxterms

2) In a computer instruction format the instruction length and size of the address field are 11 & 4 bits respectively. A computer architect has already designed 6 two address & 24 zero address instructions. What is the maximum number of 1 address instructions that can be added to the instruction set? (10)

3) Using a 4 - bit CLA as the building block, design the fastest 64 - bit adder. Estimate the add time of your design. (10)

4) Design a 4 - bit general purpose register to perform the following function (10)

S1	S0	FUNCTION
0	0	Load external data
0	1	Rotate left ($A_3 \leftarrow A_0$, $A_i \leftarrow A_{i-1}$ for $i = 1, 2, 3$)
1	0	Rotate right ($A_0 \leftarrow A_3$, $A_i \leftarrow A_{i+1}$ for $i = 0, 1, 2$)
1	1	No operation

5) Explain the Booth's algorithm for multiplication of two numbers represented in 2's complement validate to perform (10)
for 3 x (-3)

6) Consider the following register transfer description. (10)

```
Declare registers    A [8], B [8], C [8], N [4];
Declare bus          Outbus [8];
START:               A ← 1, B ← 1, C ← 0; N ← 10;
                     Outbus ← A;
LOOP:                Outbus ← B;
                     If N = 0 then go to HALT;
                     C ← A + B;
                     A ← B;
                     B ← C;
                     N ← N – 1;
                     Go to LOOP;
HALT:                HALT
```

Propose a block schematic of the optimized microprogrammed control unit; provide the state diagram and obtain the control words required in the optimized control memory.

7) Explain the different operating modes of ARM7. (10)

8) Explain following instructions with an example to each instruction (5 x2) (10)

Load/store
Load/store halfword
Load/store byte
Load/store signed byte
Load/store signed halfword

9) Explain the working of following instructions: (5 * 2 = 10) (10)
a) STMIA r0!, {r2, r3, r4} b) ADDEQ r0,r1,r2,LSR#2 c) MRS CPSR,r0
d) MOV PC,r14 e) BIC r0,r1

10) Write a short note on ASB bus. (10)

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