Question Paper

Exam Date & Time: 24-Nov-2018 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

SCHOOL OF INFORMATION SCIENCES

FIRST SEMESTER MASTER OF ENGINEERING - ME (VLSI DESIGN)

High Level Digital Design [EDA 611]

Marks: 100 **Duration: 180 mins.**

END SEMESTER DEGREE EXAMINATION NOVEMBER 2018

Answer all the questions.

1) Implement the F = $\sum$WXYZ(0, 2, 5, 7, 9, 11, 12, 15) logic function using multiplexer (10)

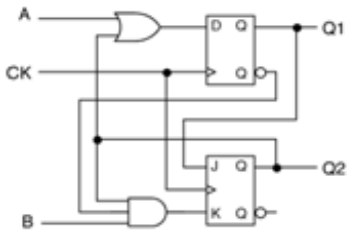
2) Design and explain the following with neat diagram (10)
a. D-Latch
b. D-FlipFlop
c. Scan D-FlipFlop

3) Design a 1101 sequence detector using Moore Machine (10)

4) Design the following (10)
a. All 0's Detector
b. All 1's Detector
c. Equality Comparator

5) Explain Carry Select Adder with neat diagram (10)

6) For the given circuit, determine the delay of the longest path. (10)



	t_P	t_{su}
D Flip-Flop:	20 ns	5 ns
JK Flip-Flip:	25 ns	10 ns
AND Gate:	12 ns	
OR Gate:	10 ns	

7) Design a Synchronous FIFO (10)

8) Explain the following (10)

a. Single Ended I/O

b. Differential Ended I/O

9) Brief explain the Split & retry operation (10)

10) Design Real Time Clock with following features (10)
a. Display - Hr : Min : Sec
b. Clock freq 500 KHz

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