Question Paper

Exam Date & Time: 27-Nov-2018 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

SCHOOL OF INFORMATION SCIENCES

FIRST SEMESTER MASTER OF ENGINEERING - ME (VLSI DESIGN)
Verification [EDA 617]

Marks: 100 **Duration: 180 mins.**

END SEMESTER DEGREE EXAMINATION NOVEMBER 2018

Answer all the questions.

1) Discuss the different verification challenges. (10)

2) What is Verification? What is being Verified in following Verification Processes (10)

a. Formal Verification
b. Functional Verification

3) Explain the following verification types (10)

a. Black Box Verification
b. White Box Verification

4) Explain randomization in SystemVerilog with example (10)

5) Write a Verilog code for 4-bit ALU? Write a Self Checking TestBench for above code. (10)

6) Describe the Architecture of Test Bench with neat diagram (10)

7) What is code coverage? Explain different types of code coverage's? (10)

8) Describe interface block in SystemVerilog and mentions its advantages (10)

9) Explain the following with example (10)

a. Inheritance
b. Polymorphism

10) Explain the following arrays in SystemVerilog with examples (10)

a. Dynamic Arrays
b. Associative Arrays

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