Question Paper

Exam Date & Time: 20-Nov-2018 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

SCHOOL OF INFORMATION SCIENCES

SECOND SEMESTER MASTER OF ENGINEERING - ME (VLSI DESIGN)

Low Power VLSI Design [EDA 608]

Marks: 100 **Duration: 180 mins.**

DEGREE EXAMINATION NOVEMBER 2018

Answer all the questions.

1) Why has low power become an important issue in the present-day VLSI circuit realization? (10)

2) What are the types of power dissipation is observed in a VLSI chip? Describe dynamic power dissipation components briefly. (10)

3) Explain combining of Parallelism with Pipelining techniques to achieve low power dissipation. (10)

4) What are the challenges in Multilevel Voltage Scaling? Explain Low to High and High to Low voltage converters. (10)

5) A battery-operated 65nm digital CMOS device is found to consume equal amounts (P) of dynamic power and leakage power while the short-circuit power is negligible. The energy consumed by a computing task, that takes T seconds, is 2PT. (10)
Compare the below two power reduction strategies for extending the battery life:
a.Clock frequency is reduced to half, keeping all other parameters constant.
b.Supply voltage is reduced to half. This slows the gates down and forces the clock frequency to be lowered to half of its original (full voltage) value. Assume that leakage current is held unchanged by modifying the design of transistors.

6) Explain gated clock Finite State Machines and Finite State Machine partitioning to achieve low power dissipation in an Integrated Circuit (10)

7)	Explain transistor stacking and multiple threshold CMOS circuit techniques to achieve low power dissipation.	(10)
8)	Explain dynamic Vth technique with the help of a diagram.	(10)
9)	Describe different types of Power Gating and its issues.	(10)
10)	Explain phase assignment and algebraic transformations in the context of low power VLSI techniques.	(10)

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