Question Paper

Exam Date & Time: 22-Nov-2018 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

SCHOOL OF INFORMATION SCIENCES

SECOND SEMESTER MASTER OF ENGINEERING - ME (VLSI DESIGN)

Universal Verification Methodology [EDA 610]

Marks: 100 **Duration: 180 mins.**

END SEMESTER DEGREE EXAMINATION NOVEMBER 2018

Answer all the questions.

1) Explain the functionality of following components with example. (10)

a. Monitor
b. Scenario Generator

2) Explain Arrays in SystemVerilog. (10)

3) Explain the functionality of following with example (10)

a. Encapsulation
b. Polymorphism

4) Explain the functionality of following with example (10)

a. uvm_object class
b. uvm_component class

5) Explain the functionality of following (10)

a. Block level environment
b. Integration level environment

6) Explain different components in UVM Testbench. (10)

7) Illustrate UVM Factory coding convention 2 and convention 3 with example. (10)

8) Explain about UVM factory overrides. (10)

9) Write a note on creation of transaction using uvm_sequence with an example. (10)

10) Explain the functionality of uvm_driver with example. (10)

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