Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

V SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2018

SUBJECT: COMPUTER ARCHITECTURE [CSE 3101]

REVISED CREDIT SYSTEM
(19/11/2018)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. With the help of neat diagrams, explain the data flow in the sub cycles, that occurs after instruction *j* is executed and before the execution cycle of instruction *k* is initiated. **3M**

```
i: DADDU R1, R2, R3      ; DADDU: adds two unsigned values
j: INT 21h               ; interrupt service routine starts from address m
k: LW R4, 0(R1)          ; LW: load word
```

1B. A pipeline consists of 5 stages S_1, S_2, S_3, S_4 and S_5 with feed forward and feedback connections in addition to the streamline connections. The stage S_i is fed forward to the stage S_j such that $j>i+2$ and it is fed back to the stage S_j such that $j<i-2$. S_1 is the input and S5 is the output stage of the pipeline. Draw the block diagram of this pipeline. Write the reservation table for the above pipeline if feedback and feed forward connections are the only connections that must be used after each clock cycle. If the total evaluation time is 6 clock cycles then, **5M**

i) List the set of forbidden and permissible latencies and the collision vector.
ii) Draw a state transition diagram showing all possible cycles without causing the collision in the pipeline.
iii) List all the simple cycles and identify the greedy cycles among the simple cycles. What is the MAL of this pipeline?
iv) What is the efficiency of this pipeline if it uses a constant cycle?

1C. Consider a four-segment linear pipeline processor with a 10ns clock period. Find the minimum number of periods required for 99 instructions, which use pipeline processor. Find the efficiency, throughput and speedup of a four-segment linear pipeline over an equivalent non-pipeline processor. **2M**

2A. Design a single stage PM2I ring network choosing a valid number of PEs such that $5 < N < 30$, where N is the number of PEs. Prove that: **5M**

i) For a single stage PM2I network the minimum number of recirculation B is upper bounded by $B \leq \frac{\log_2 N}{2}$.
ii) The PM2I network is faster than the Illiac Network.

2B. Design a Multistage Network that has 4, 2X2 switches in each stage and uses Inverse-Shuffle routing function between the stages. The PEs are directly connected to the switch boxes on the input side. Solve the routing functions by considering all the PEs and write the corresponding permutation cycles. Show the switch settings in the above design for routing a message from PE_0 to node PE_6. How do you achieve this path? **5M**

3A. Draw a neat diagram of Intel's product that has shared L2 cache. Explain the features provided in this product with respect to the shared L2 cache unit. **4M**

3B. Compare shared L2 cache on the chip over dedicated L2 caches in the multicore system. **3M**

3C. Explain the organizational changes involved in processor design to increase instructional level parallelism. Explain the power consumption issues with respect to these designs and how is it overcome? **3M**

4A. A SMP system contains three processors with L2 caches connected to a time-shared bus as shown in Figure 4A. Considering the scenario given below draw the block diagram before and after the state change for the following two cases by taking appropriate values for the variables. (M – Modified, S – Shared and I – Invalid) **5M**

i) In Processor B's L2 cache state of X changes from M to S
ii) In Processor C's L2 cache state of Y changes from M to I

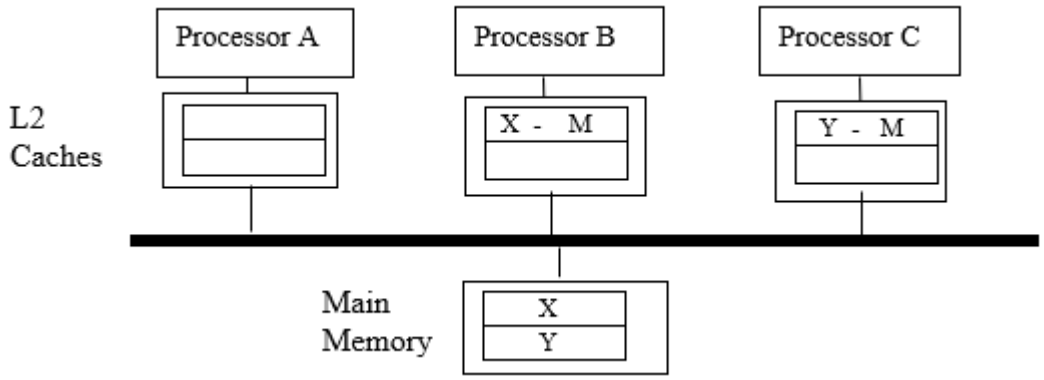

Figure 4A: SMP system

4B. Explain the characteristics of a process. Does process switch consume less time than thread switch? Justify your answer. **2M**

4C. With a neat diagram for each explain the different approaches of multithreading in a scalar pipeline architecture and the pipeline architecture that have hardware for issuing four instructions per cycle but only instructions from a single thread are issued in a single cycle. **3M**

5A. List and explain the clustering methods with their advantages and disadvantages respectively. **3M**

5B. With a neat diagram explain the cluster architecture and the services that provide a single system image. **4M**

5C. Give a comparison between clusters and simultaneous multithreading. **3M**