Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

V SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

MAKE-UP EXAMINATIONS, DEC 2018/ JAN 2019

SUBJECT: COMPUTER ARCHITECTURE [CSE 3101]

REVISED CREDIT SYSTEM
(21/12/2018)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. With a neat space-time diagram explain and derive the speed up of a linear pipeline processor over a non-pipeline processor. **3M**

1B. Explain the four programmatic levels in parallel processing with example. **2M**

1C. Design an Omega Network which has 4, 2X2 switch boxes in each stage. Solve the routing functions by considering all the PEs and write the corresponding permutation cycles. Show the switch settings in the above design for routing a message from PE_0 to node PE_6. Find another source and destination which creates a block in the above path and show the corresponding switch settings. **5M**

2A. Consider the three staged pipeline processor specified by the following reservation table 2A. **2M**

Table 2A. Reservation table

	1	**2**	**3**	**4**
S1	X			X
S2		X		
S3			X	

i) List the set of forbidden and permissible latencies and collision vector

ii) Draw a state transition diagram showing all possible cycles without causing the collision in the pipeline

2B. Design a pipeline that adds two normalized floating-point numbers A = a *x* 2^p and B=b *x* 2^q where a and b are fractions and p and q are their exponents respectively. What are the operations performed by the different stages of this pipeline? **4M**

2C. Find the sum of the numbers given below using an array of 16 PEs. Show the contents of the PEs in each step. Write the algorithm and the masking scheme for the same. **4M**

12 23 21 43 21 13 15 4 6 10

3A. What are the variables in a Multicore organization? With neat diagrams explain the general organizations for multicore systems. **5M**

3B. With a neat diagram explain all the features of an Intel's product having shared L3 cache organization. **3M**

3C. Why the software performances force Multicore systems as an alternative to the Multiprocessor systems? **2M**

4A. A SMP system contains three processors with L2 caches connected to a time-shared bus as shown in the Figure 4A. Considering the scenario given below draw the block diagram before and after the state change for the following two cases by taking appropriate values for the variables. (M – Modified, I- Invalid and S – Shared) **5M**

i) In Processor A's L2 cache state of X changes from S to M

ii) In Processor B's L2 cache state of Y changes from M to I

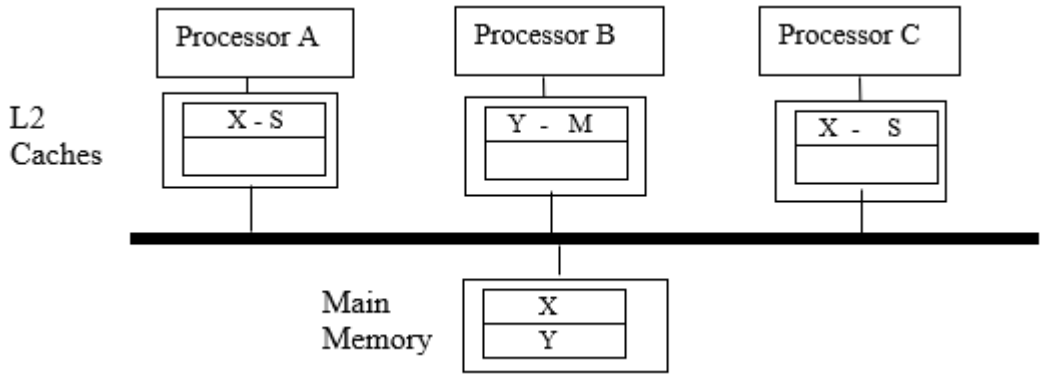

Figure 4A. SMP System

4B. Explain how the consistency is maintained between L1 and L2 cache. **2M**

4C. Explain how the distributed hardware approach distributes the responsibility to maintain the cache coherency in simultaneous multiprocessors. **3M**

5A. What is explicit multithreading? List and explain the different approaches to explicit multithreading. **3M**

5B. Explain the different cluster configurations with a neat diagram for each. What are the benefits of clustering? **4M**

5C. In a cluster configuration, how are the load balancing and failure management handled? **3M**