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# MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
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**FIFTH SEMESTER B.TECH. (E & C) DEGREE END SEMESTER EXAMINATION**
**NOVEMBER 2018**
**SUBJECT: COMPUTER ORGANIZATION AND ARCHITECTURE (ECE - 3106)**

**TIME: 3 HOURS** **MAX. MARKS: 50**

**Instructions to candidates**
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Draw the organization of register based machine. For the given expression $Y=(A+B-C)/(D*E/(F+G))$ write the optimized code for the above machine having a restriction that the destination operand must be a register. Write another version for the same without using any registers. Compare these two programs with respect to the following parameters.

a. Number of instructions b. program size (bytes)
c. Number of distinct registers d. number of memory accesses for operands

Assume that the memory address is of 16-bits, register address is of 3-bits and opcode is of 8-bits in length. Write your comments for the comparative analysis

1B. In a computer instruction format, the instruction length and size of the address field are 11-bits and 4-bits respectively. The instruction set has 6 two address and 24 zero address instructions. Using expanding op-code technique, compute the number of one address instructions that can be added to the instruction set.

1C. Convert the following decimal numbers to equivalent 32-bit IEEE floating point representation.

a. 45.125 b. – 0.0125

(4+3+3)

2A. Using 4-bit CLA as a building block design a 16-bit adder. Use this 16-bit adder as a building block to design a fastest 64-bit adder. Estimate the worst case add time of your design.

2B. Design an array (Braun's) multiplier for multiplying two 4-bit numbers.
Assume that $\Delta_{\text{AND gate}} = \Delta$carry propagation=2 gate delays =2Δ, what is the total delay?

2C. Design and implement a digital circuit using parallel adder and 2:1 MUX that will work as follows: Assume A is 4-bit data:

| S1 | S0 | Function F |
|---|---|---|
| 0 | 0 | *Shift left* (A) |
| 0 | 1 | (1111)b |
| 1 | 0 | *Shift left* (A) plus 1 |
| 1 | 1 | (0000)b |

(4+3+3)

3A. Using the algorithm given below draw the processing section by showing all the necessary control signals for the 4X4 unsigned multiplier. Design a Micro-Programmed Control unit for the same. Give the binary listing of the microprogram.

Declare registers A[4], M[4], Q[4], L[3], Inbus [4], Outbus[4]
START: A← 0, M←Inbus, L←4;
Q← Inbus;
LOOP: If Q[0]=1 then A←A+M;
RSHFT (A$Q), L←L-1;
If L< > 0 then go to LOOP
Outbus←A;
Outbus←Q;
HALT: Go to HALT

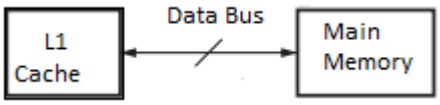
3B. Build the hardware to implement each of the following register transfers:
i) If Q[1]=0 and Q[0]=1 then A←A+1 else A←A-1
ii) If Q[1:0]=01 OR Q[1:0]=10 then A←B
Assume A, B and Q are 4-bit registers.

3C. Write the RTL code of Booth's Multiplication procedure.

(4+3+3)

4A. Explain with the neat diagrams, different ways to handle multiple interrupts from several I/O devices. Consider in an industry environment 3 parameters namely pressure, smoke and humidity are to be monitored. These analog sensors are interfaced with a microprocessor through INT and INTA pins. Implement a relevant I/O diagram by assigning the priority.

4B. Show the memory hierarchy organization of a computer system. Derive the expression for efficiency of a memory system. The access time of main memory is 10 times that of cache memory access. Compute the hit ratio if average access time is 100ns and efficiency is 0.8.




4C. Consider the hexadecimal main memory address ABCD9987 and size of the cache is 64KB. Assume line (block) size is 128 Bytes. Find the i) cache line number and word number in direct mapping. i) SET number and the TAG value if 4 lines are made as one set (4 blocks per set).

(4+3+3)

5A. Discuss the following terms in the context of pipelining:
i) cycle time ii) latency iii) performance.
Write the different pipeline hazards which limit the performance of a processor. Give suitable examples with respect to 5-stage pipeline.

5B. Explain the following architectures in brief : i) OMAP ii) VLIW iii) DSP

5C. Compute the sequence in which the input data should be ordered for a 16 point DIT FFT using bit reversed addressing mode. Give the table.

(4+3+3)