Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
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A Constituent Institution of Manipal University

FIFTH SEMESTER B.TECH. (E & C) DEGREE END SEMESTER EXAMINATION
DECEMBER 2018/JANUARY 2019
SUBJECT: COMPUTER ORGANIZATION AND ARCHITECTURE (ECE - 3106)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Describe stack based computing machine using a neat block diagram. Explain how it can be used for computing the following expression, $Y = (A - B) * (C + D)$ showing the stack contents while it is getting executed. Give the RPN format for the same.

1B. Given the symbol probabilities, g0 = 0.22, g1 = 0.34, g2 = 0.17, g3 = 0.19 and g4 = 0.08. Perform encoding for the symbols using Huffman's encoding. What's the average length of the bits? Find redundancy and efficiency of the method.

1C. Convert the IEEE floating point number 43A4B200h to decimal value.

(4+3+3)

2A. Draw a 4-bit ripple carry adder using FA blocks. Assuming two and three gate delay for getting carry and sum respectively for every FA block, find the delay involved in generating final sum. Explain how CLA will improve the speed of the above adder.

2B. Perform multiplication on -74 X 52 using Booth's algorithm. Show all the iterations. Verify your answer using Bit pair recoding method. Write how many iterations may be needed in the second method?

2C. Design a 4-bit general purpose register for a given input as X, for the following functions:

S1	S0	Function (Y)
0	0	Decrement X
0	1	Arithmetic right shift X
1	0	2X
1	1	Rotate left X

(4+3+3)

3A. Design a hard wired controller for the 4X4 unsigned multiplier.

3B. Design an arithmetic unit for the specifications given in Table 3B. A and B are 4-bit data.

3C. Build hardware to implement each of the following register transfers:

i) If C[1]=0 and C[0]=1 then A←A+B else A←A-B

ii) If C=B and D[1]=1 then A←B

Assume A, B, C, D are 4-bit registers.

(4+3+3)

4A. Explain programmed I/O approach for I/O communication. Explain its disadvantages. Discuss the approach as which will alleviate its disadvantages.

4B. A block set associative cache consists of a total of 64 blocks divided into 4 block sets. The main memory contains 4096 blocks each containing 128 words.

a) How many bits are there in main memory address?

b) How many bits are there in each of the TAG, SET & word fields? Show the address format

c) If we use fully associative mapping, show the address format with TAG and word fields.

4C. Explain the virtual memory concept. Consider a logical address space of 32 pages of 1024 words mapped onto a physical memory of 8 frames. How many bits are in a virtual address and physical address?

(4+3+3)

5A. Explain a 5 stage instruction pipeline with diagram. Derive the expression for average number of instruction executed per instruction cycle.

5B. Explain the following architectures i) VLIW ii) RISC

5C. A DSP has a circular buffer with start and end addresses as 0400h and 040Fh, respectively. What would be the new values of address pointer of the buffer if updated to i) 0412H, ii) 03FCH in the course of address computation.

(4+3+3)

Table 3B

S_2	S_1	S_0	Function F
0	0	0	A
0	0	1	A’
0	1	0	A *plus* B
0	1	1	A *plus* B’
1	0	0	A *plus* 1
1	0	1	A’ *plus* 1
1	1	0	A *plus* B *plus* 1
1	1	1	A *plus* B’ *plus* 1