MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

FIFTH SEMESTER B.TECH. (E & C) DEGREE END SEMESTER EXAMINATION
NOVEMBER 2018
SUBJECT: MICROCONTROLLERS (ECE - 3102)

TIME: 3 HOURS   **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A.   Describe all the addressing modes supported by 8051 with suitable examples.

1B.   Write differences among the following:
i. RISC and CISC architecture
ii. Harvard and Von-Neumann architecture
iii. SRAM and DRAM

1C.   With neat diagram describe the internal data memory organization in 8051.

                                                                        4+3+3

2A.   A Metro Railway station has a number of self-operated ticket purchase counters. Assume that there are 16 stations in the Metro which are precoded from 0 to F_h keys of the 4X4 keyboard. Passenger has to enter source station code followed by destination station code. The system has to calculate the journey fare using **Table 2A** and display the fare on the LCD module in the following format: Fare: Rs…………..
   A. Draw the neat interface diagram showing all connection
   B. Write an 8051 Assembly language program to implement the task (Fare related data is given in **Table 2A**)

2B.   Write an 8051 assembly language program to calculate Z based on the following equation and store the result in internal data memory 60H(Quotient) and 61H(Remainder):
$$Z= (X+Y)/(X-Y)$$
Assume that X, Y, Z, X+Y, X-Y are 2-digit BCD numbers and X greater than Y.
X and Y stored in internal data memory 50H and 51H

                                                                        6+4

3A.   Describe the functions of each bit in the following SFRs with bit diagram:
i. TCON   ii. SCON   iii. PSW   iv. IP

3B.   Interface an 8-bit ADC and stepper motor to 8051. Design a system that can sense an analog voltage from 0 to +5V and control the stepper motor. Draw a neat interface diagram and write an assembly language program to rotate the stepper motor clockwise as long as analog input voltage is less than +2V and rotate it anti-clockwise if input exceeds +2V.

3C.   Explain briefly the following instructions of 8051 with syntax
          i. DA   ii. RRC   iii. XCHD

                                                                        4+3+3

4A. Write an 8051 assembly language program using interrupts to do the following
i. Receive data serially and send it to P0,
ii. Have P1 port read and transmitted serially, and a copy given to P2
iii. Make timer0 to generate a square wave of 5KHz frequency on P3.1
Assume that XTAL=11.0592MHz, Set the baud rate at 4800.

4B. Write the 3-stage pipeline (as per ARM7) execution flow of the following sequence of instructions till 8 clock cycles.

```
        MOV r2, #8
        ADD r1, r3, r3, LSL #1
        B L2
        SUBS r4, r4, r2
        EORS r1, r3, r4
        MOV r2, #5
    L1: B L1
    L2: MUL r3, r2, r2
        ANDS r5, r3, r0
        MOV PC, LR
```

4C. Draw the neat unsigned byte/word data transfer instruction format and explain each field in the of ARM processor.

4+3+3

5A. Explain the ways in which ARM instruction set differs from pure RISC definition to suit for embedded applications.

5B. Given r0=0x800C0077, r1=0x00C08090, r2=0x61209000, r3=0x00000002. What would be the content of r0 and r1 after executing below ARM instructions
    i. BIC r0, r1, r2   ii. RSB r0, r1, r2   iii. UMULL r0, r1, r2, r3
    iv. MLA r0, r2, r3, r1   v. MVN r0, r1, LSL #1   vi. EOR r0, r1, r2, LSL r3

5C. With neat bit format, explain the function of each bit in the CPSR register of ARM processor

4+3+3

Table 2A			
Difference between Station numbers	Fare (Rupees:Paise)	Difference between	Fare (Rupees:Paise)
1	10:00	9	30:00
2	12:00	10	32:00
3	15:00	11	35:00
4	17:00	12	37:00
5	20:00	13	40:00
6	22:00	14	42:00
7	25:00	15	45:00
8	27:00		
14	42:00		
15	45:00		