Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FIFTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION
DECEMBER 2018/JANUARY 2019
SUBJECT: VLSI DESIGN (ECE - 3104)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Find the optimal number of **NMOS** inverters to be cascaded so as to drive load capacitance of 1.48 pF off-chip capacitive load such that the total delay is minimized.
Given that $1\square C_g$ = 0.01pF. Give the cascaded structure with L:W ratios. Find the overall delay T_d showing the delay across each inverter stage.

1B. Give the block level implementation of the design of 2-bit Twisted Ring counter using shift register stages with two phase non-overlapping clock. Given that shift register stages have parallel load feature.

1C. Estimate the CMOS inverter pair delay for the circuit arrangement shown in Figure 1C for the rising and falling input. Given that $R_n=R_p=1R_s$ and INV2 drives the capacitive load that is equal to capacitive load seen by INV1.

(3+3+4)

2A. i. Prove that NMOS inverter is ratioed logic. How Voltage-Transfer-Characteristic (VTC) of NMOS inverter varies with Zpu/Zpd ratio.
ii. Draw the stick notation for ACT-1 MODULE.

2B. Explain the operation of the N-bit parity generator.

2C. An NMOS device is plugged into the test configuration shown below in Figure 2C. The input Vin =2V. The current source draws a constant current of 50 μA. R is a variable resistor that can assume values between 10kΩ and 30 kΩ. Transistor M1 experiences short channel effects and has following transistor parameters: $\mu_n C_{ox}= 110*10^{-6}$ V/A^2, V_T = 0.4 , and $V_{d,SAT}$ = 0.6V. The transistor has a W/L = 2.5μ/0.25μ. For simplicity body effect and channel length modulation can be neglected. i.e λ=0, γ=0.
i. When *R* =10kΩ find the operation region, V_D and V_S.
ii. When R= 30kΩ again determine the operation region V_D, V_S
iii. For the case of R = 10kΩ, would V_S increase or decrease if $\lambda \neq 0$. Explain qualitatively.

(3+3+4)

3A. Explain the fabrication process of twin-tub CMOS with neat diagram.

3B. Explain the structure design of N-bit bus arbitration logic. Draw the layout of one cell/bounding box also.

3C. i. What is the effect of combined E model on gate oxide thickness and gate area?

ii. Explain the operation of circuit shown in Figure 3C. Is it ratioed or ratioless?

(3+3+4)

4A. Implement the function $F = \overline{AB + CD}$ using dynamic logic and explain its operation. Explain the charge leakage issue in the circuit and remedy for that?

4B. i. For the given example of capacitive coupling metal 1 wire X and polysilicon wire Y has parasitic coupling capacitance of C_{XY} = 0.5fF. Wire Y has C_Y = 6fF. If the node X takes a step transition of 0-2.5 V find the voltage drop in floating line Y.

ii. Draw the stick diagram of MUX based D-latch.

4C. Briefly explain the read and write modes of operations of 6T SRAM cell. Draw the stick diagram of 6T SRAM cell and sense amplifier used during read operation.

(3+3+4)

5A. Consider the following MOSFET as shown in Figure 5A, where we are using 65nm technology with supply voltage V_{DD} = 1.2 V and threshold voltage V_{TP} = -0.3 V. Furthermore, assume that the surface mobility is 200 cm^2/Vs, C_{ox} = $19*10^{-7}$ F/cm^2 and that W/L = 3. Finally, V_S is the voltage supplied to the source, V_G is the voltage applied to the gate, and V_D is the voltage at the drain of the MOSFET.

i. Suppose V_S = 1.2 V, V_G = 0.1 V, and V_D = 0.5 V. Calculate the drain current.

ii. Suppose V_S = 1.2 V, V_G = 0.8 V, and V_D = 0.1 V. Calculate the drain current.

5B. What is Electro-migration? Explain electro migration related failure modes.

5C. Draw the layout of 3T DRAM shown in Figure 5C.

(3+3+4)

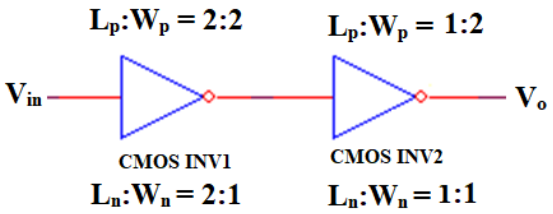

Figure 1C

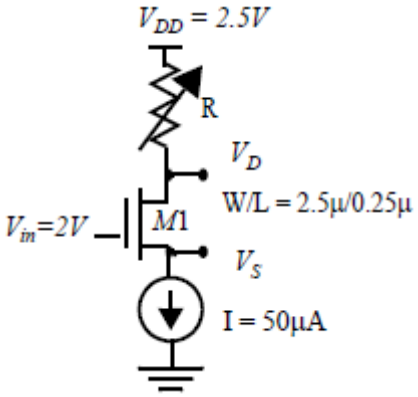

Figure 2C

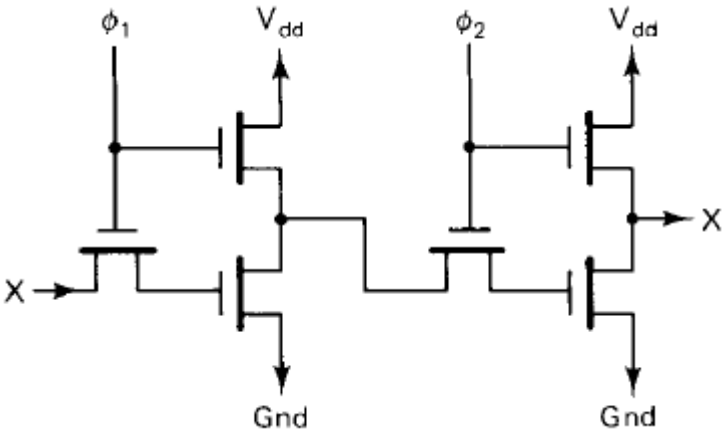

Figure 3C

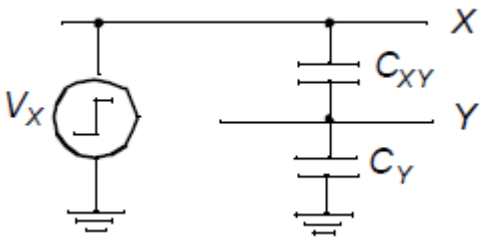

Figure 4B

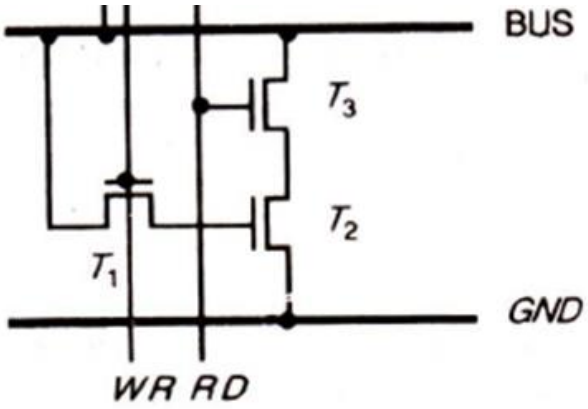

Figure 5C

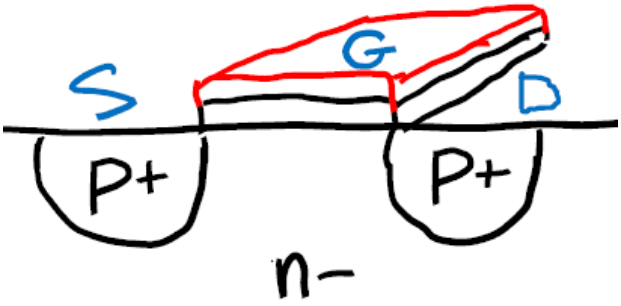

Figure 5A