Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FIFTH SEMESTER B.TECH. (E & C) DEGREE END SEMESTER EXAMINATION
NOVEMBER 2018
SUBJECT: VLSI DESIGN (ECE - 3104)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. i. Define sheet resistance.

ii. Calculate the input capacitance C_{in} for the Layout shown in Fig. 1A. Note that the input capacitance C_{in} is the total capacitance between metal and ground. Refer the Table. 1A for typical values of area capacitance for 5 µm technology.

1B. Give the circuit implementation of following multiple output function using Pseudo-NMOS NOR-NOR based PLA. $Y_1 = AB + A'B'C$; $Y_2 = AB + B'C$; $Y_3 = A + B'C$

1C. i. Give the mathematical expression for 'channel length modulation parameter'.

ii. For a given enhancement mode NMOS transistor biased in saturation region, I_{ds}=1mA, V_{ds}=5V. When V_{ds} was increased to 6 V while keeping gate source voltage constant, the I_{ds} increased to 1.02 mA. Assume that drain-to-source saturation voltage is much smaller than the applied drain source voltage. Find the value of channel length modulation parameter.

(3+3+4)

2A. i. Calculate the power dissipated in the inverter circuit shown in Fig. 2A for Vi=0.25 V and Vi=4.3 V. Given, **β_L= 10 µA/V^2, β_D= 100 µA/V^2.**

ii. Draw the stick of 1-bit cell of binary to gray converter.

2B. Draw the layout of one cell of 4x4 barrel shifter. Perform 1-bit left shift operation.

2C. Implement the following words using ROM structure and draw the stick also. The selected row for reading is selected in active low fashion. The pull-up device is PMOS and dynamic in operation.

W1=1100; W2=0011; W3=1001; W4=1110.

(3+3+4)

3A. An engineer from TSMC is experiencing the leakage current due to latch-up in standard CMOS IC. While searching for the solutions, he stumbles upon a set of files where possible solutions to leakage problem are addressed. These files contain following information

i. Silicon is epitaxially grown on sapphire or magnesium aluminate spinel.

ii. All the layers are grown onto the substrate.

iii. PMOS and NMOS transistor are fabricated into Small Island onto the substrate. Density of transistors are very high.

iv. No problem of field inversions exits.

Identify the type of MOS fabrication and explain the complete fabrication process with neat diagram.

3B. Perform following function using ALU unit and draw the stick notation of one cell.
i. 1000 **SUB** 1001 ii. 1010 **XOR** 0011 iii. 0101 **AND** 1100

3C. i. Derive the Zpu/Zpd ratio of the pseudo nmos inverter. Suggest a scheme to make it dynamic logic without changing the type of transistor.
ii. Consider the ring counter with initial content=1000. Implement the same using R/2 dynamic memory element/s.

(3+3+4)

4A. Give the optimal Domino CMOS implementation of given multiple output functions

$$C_1 = G_1 + P_1C_0 \;\; ; \;\; C_2 = G_2 + P_2G_1 + P_2P_1C_0$$

4B. i. A current level of 25 mA is supplied by a power supply (VDD) of 1.2 V and flows into the circuit over a 100 ps time interval. Calculate the total voltage drop due to the inductance on both VDD and VSS rails as shown in Fig. 4B.
ii. Draw the stick diagram of a CMOS R/2 register stage.

4C. Draw the device structure of ETOX flash cell and briefly explain the erase, read and write basic operations of NOR flash memory.

(3+3+4)

5A. Various NMOS and PMOS transistors numbered from 1 to 3 are measured in an operation as shown in the Table 5A. For each transistor, find the value of $\mu CoxW/L$, type, mode and complete the table with V in volts, I in μA, and $\mu CoxW/L$ in $\mu A/V^2$. Given, Vt(NMOS)=0.5 V, Vt(PMOS)= -0.5 V. Type= NMOS or PMOS, Mode=cut-off, saturation or linear.

5B. Today's technology demand IC packages of 5000 pins. The simultaneous switching of a lot pads, each driving a large capacitor, causes large transient currents and creates voltage fluctuations. In order to overcome these, Engineer's from INTEL has come to design an output stages of buffer. The design is as follows:
The IC's (CMOS based) on-chip minimum size inverter has to drive an off-chip capacitor C_L = 10 pF in 1.2 um technology (□Cg=0.0023 pF). What will be the Engineer's calculation for:
i. Number of stages ii. Total delay iii. Ratio of each stage.

5C. Draw the layout of the Dynamic CMOS function of $F = \overline{AB + CD}$. $\beta_n \neq \beta_p$

(3+3+4)

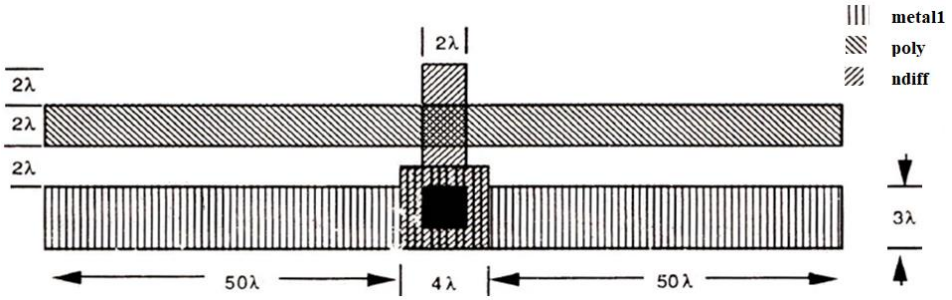

Fig. 1A

Table 1A

Capacitance	Value in pF*/ micromt² (relative values in brackets)
Gate to channel	4 (1.0)
Diffusion	1 (.25)
Poly to sub	0.4 (.1)
M1 to sub	0.3 (0.075)
M2 to sub	0.2 (0.05)
M2 to M1	0.4 (0.1)
M2 to poly	0.3 (0.075)

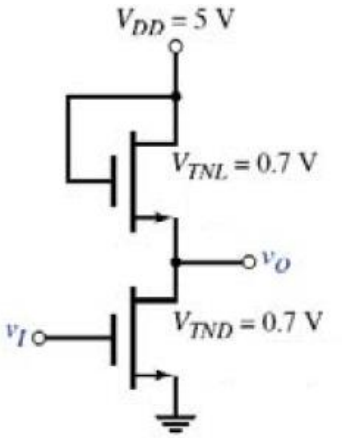

Fig. 2A

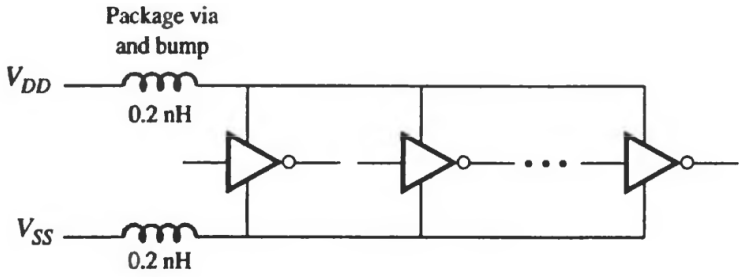

Fig. 4A

Table 5A

Case	Transistor	Vs	Vg	Vd	Id	Type	Mode	μ*CoxW/L*
A	1	0	2	5	100			
	1	0	3	5	400			
B	2	5	3	-4.5	50			
	2	5	2	-0.5	450			
C	3	-2	0	0	72			
	3	-4	0	-3	270			