Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent Institution of MAHE, Manipal)

VII SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, NOVEMBER 2018

SUBJECT: EMBEDDED PROCESSOR ARCHITECTURE [ELE 4003]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 27, November 2018** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Explain the different Architectural style and describe the advantages / disadvantages of load-store architecture? ***(05)***

1B. Define and explain the different dependencies exhibit by following code and explain how it can be overcome

```
MOV R7,R3
ADD R7,R7,#2
LOAD R8,[R7]
ADD R3,R3,#4
LOAD R9,[R3]
BNE R8,R9,L3
```

(03)

1C. Explain the Instruction Level Parallelism (ILP) foundation for the Embedded system Architecture ***(02)***

2A. Explain the 5-Stage organization of ARM9TDMI ,describe the Behavior of Program counter (PC)to emulate the Behaviour of 3- stage ARM pipeline in same Architecture ***(02)***

2B. Write the pipeline structure for the 5-stage ARM core following code ,explain which instruction causes stall ,calculate CPI and define type of Hazard

```
LDMIA R13!,{R0-R4}
SUB R9,R7,R3
STR R4,[R9]
ORR R8,R4,R2
AND R6,R2,R1
```

(04)

2C. What are the significance of pipeline registers and explain the different control signals associated pipeline implementation ***(04)***

3A. With neat diagram explain the Two-level virtual-to-physical address translation using coarse page tables ***(04)***

3B. Describe the Memory Protection Unit implemented in ARM Architecture ARM940T ***(04)***

3C. Write the assembly code and steps to involved in initializing the instruction TCM in ARM946E-S ***(02)***

4A. With Neat diagram explain the 5 stage pipeline architecture of ARM9ES and describe the different architectural support for ARM5VTE instruction set ***(05)***

4B. Draw the neat diagram and explain the two scheduling algorithms implemented in ARM architecture. ***(05)***

5A. Draw Advanced High Performance Bus (AHB) interconnection diagram and explain the significance of multiplexer interconnect scheme ***(04)***

5B. Explain the Significance Floating point Unit (FPUs) in ARM Digital Signal Controllers (DSCs) ***(02)***

5C. Explain the different ARM SIMD instructions specifically used for DSP application ***(04)***