Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent Institution of MAHE, Manipal)

VII SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

MAKE-UP EXAMINATIONS, DECEMBER 2018

FPGA BASED SYSTEM DESIGN [ELE 4002]

REVISED CREDIT SYSTEM

Time: 3 Hours **31 December 2018** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Compare between the design of electronic circuits for a specific application using ASIC and programmable ASIC approach. ***(02)***

1B. With help of flow diagram explain the partial reconfiguration design flow in case of FPGA based system design. Highlight the significance of each step. ***(04)***

1C. Determine the minimum set of test-vectors required to test s-a-0 and s-a-1 faults at all points in the circuit shown in Fig. Q1C. ***(04)***

2A. An 8:1 multiplexer with an active high enable is to be implemented using Xilinx SPARTAN-II E FPGA with the following options

i. Only LUTs

ii. LUTs and dedicated expansion multiplexers

Draw its circuit schematic specifying the contents of the LUTs. How many CLBs are needed for the implementation in each case? ***(04)***

2B. Draw and explain the transmission gate based LUT. ***(02)***

2C. Explain the structure of CLB in Xilinx SPARTAN - IIE FPGA highlighting its usage. ***(04)***

3A. Draw the state diagram of logic design shown in Fig Q3A ***(04)***

3B. Develop and explain FPGA based architecture for distributed arithmetic FIR filter. ***(04)***

3C. Differentiate between fine, medium and coarse grained FPGA architectures ***(02)***

4A. Implement the following logic functions on Actel ACT-1 logic module.

i. f=a+b+c

ii. f=ab+bc+ca ***(04)***

4B. What are the benefits of using a soft embedded processor in an FPGA over a hard macro implementation? ***(02)***

4C. Write Verilog test bench code for positive edge D flip-flop. Display the message “error” if D flip-flop output is not matching with expected result. Assume Verilog code for D flip-flop is available ***(04)***

5A. Write the short notes on antifuse Programming Technology ***(03)***

5B. Draw the synthesized circuit for the Verilog code given below:

```
module q5b(
output reg [7:0] Sum,
input [7:0] A, B, C,
input clk);
reg [7:0] rA, rB, rC;
always @(posedge clk) begin
rA <= A;
rB <= B;
rC <= C;
Sum <= rA + rB + rC;
end
endmodule
```

(02)

5C. Find the distinguishing sequence for the following state table and find the inputs to verify all the transitions.

State	Next state		Output	
	X=0	X= 1	X=0	X=1
S0	S0	S1	0	0
S1	S0	S2	1	1
S2	S3	S3	1	1
S3	S2	S0	1	0

(03)

5D. Draw CMOS based logic circuit for the logic function f (x1, x2, x3) = Π(1,3, 5, 7) ***(02)***

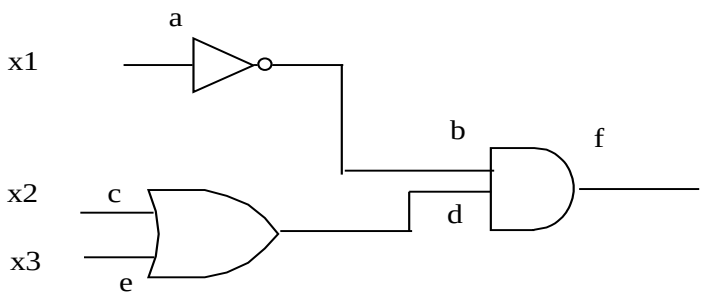

Fig Q1C

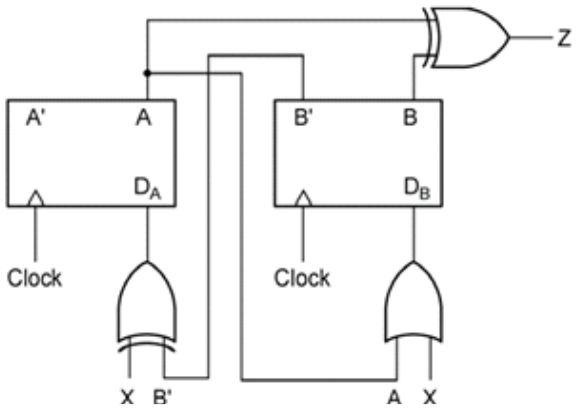

Fig Q3A