Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent Institution of MAHE, Manipal)

VII SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, NOVEMBER 2018

FPGA BASED SYSTEM DESIGN [ELE 4002]

REVISED CREDIT SYSTEM

Time: 3 Hours **29, November 2018** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Differentiate between semi-custom and full-custom design of integrated circuits ***(02)***

1B. Explain the design flow for FPGA based system design, highlighting the significance of each step. What are the advantages with FPGA based system design? ***(04)***

1C. Find a minimum set of test-vectors that will test all single stuck-at-0 and stuck-at-1 faults for the network given in Fig Q1C. For each test-vector, specify which faults are tested for s-a-0 and for s-a-1. ***(04)***

2A. Design a pseudo-random number generator with n=3 that generates a maximum length sequence. Add logic so that 000 is included in the state sequence. Determine the actual state sequence. ***(03)***

2B. With the help of block diagram explain self-test circuit for RAM ***(03)***

2C. Sketch the basic block diagram of Xilinx Spartan IIE FPGA and briefly explain the major configurable elements. ***(04)***

3A. Draw the state diagram for the serial adder shown in Fig. Q3A. Inputs to the state machine are x and y. Output is sum. ***(03)***

3B. The impulse response of a linear phase FIR filter is h(n)=[2 1 3]. Develop FPGA based architecture for distributed arithmetic FIR filter. Explain the developed architecture. ***(04)***

3C. List and explain the possible functions of DLL. What is the need for clock tree? ***(03)***

4A. A given system has three sensors that can produce an output of 0 or 1. The system operates properly when exactly one of the sensors has its output equal to 1. An alarm must be raised when two or more sensors have the output of 1. Design the simplest circuit that can be used to raise the alarm. Implement the circuit on Actel ACT-1 logic module. ***(03)***

4B. Discuss the desired features and advantages of partial reconfiguration. Mention the commercially available FPGA devices which support partial reconfiguration ***(04)***

4C. Write Verilog test bench code for two input XOR logic gate. Display the message "error" if XOR output is not matching with expected result. Assume Verilog code for XOR logic gate is available ***(03)***

5A. Write the short note on EPROM Programming Technology ***(03)***

5B. Draw the synthesized circuit for the Verilog code given below:

```
module Q5B(x, a, b, c, d);
input wire [15:0] a, b, c;
input wire d;
output reg [15:0] x;
reg [15:0] t;
always @ ( a or b or c or d ) begin
if ( d ) t = b; else t = c;
if ( a < 8 ) t = t + 12;
x = a + t;
end
endmodule
```

(02)

5C. Consider the state diagram shown in Fig.Q5C. Determine the shortest input sequence that will distinguish the state transitions. Also verify all state transitions for state B and D. ***(03)***

5D. Draw CMOS based logic circuit for the logic function f (x1, x2, x3) = ∑ (3, 4, 5, 7) ***(02)***

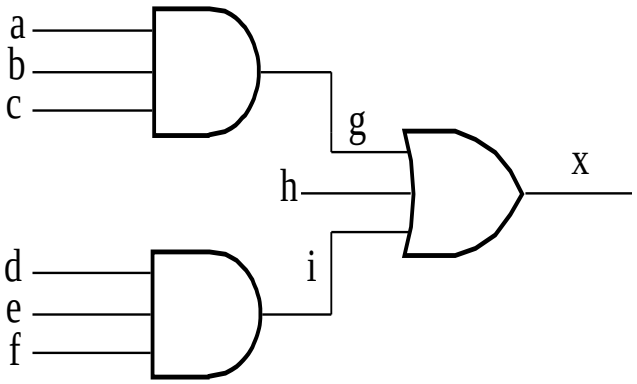

Fig.Q1C

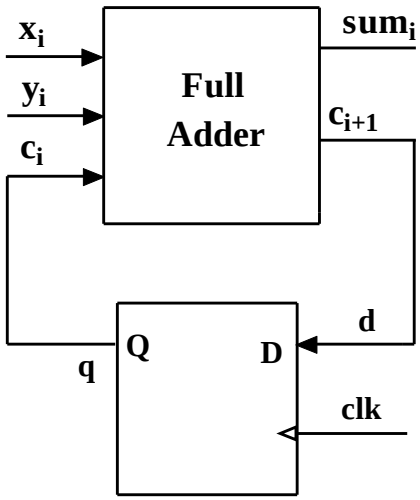

Fig. Q3A

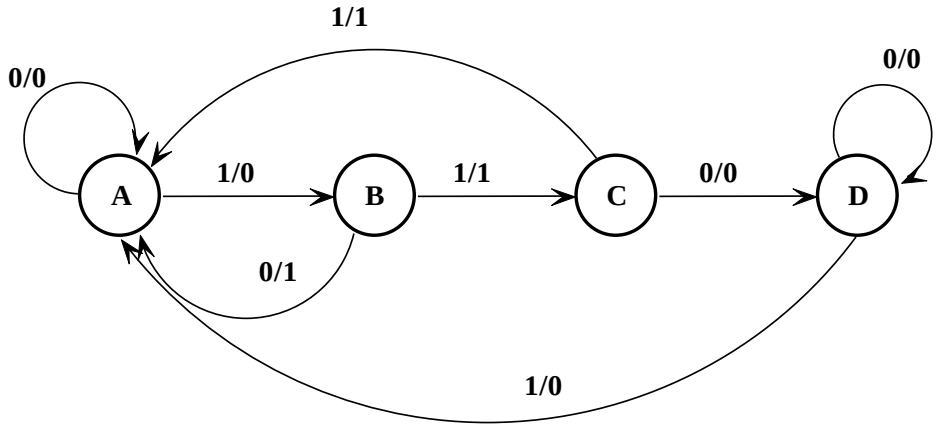

Fig. Q5C