Reg. No.



MANIPAL INSTITUTE OF TECHNOLOGY MANIPAL

(A constituent Institution of MAHE, Manipal)

VII SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING) END SEMESTER EXAMINATIONS, NOVEMBER 2018

SUBJECT: MODERN POWER CONVETERS [ELE4010]

REVISED CREDIT SYSTEM

Time: 3 Hours		Date: 24, November 2018	Max. Marks: 5	50	
Instructions to Candidates:					
	 Answer ALL the questions 				
	 Missing data may be suital 	bly assumed.			
1A.	Derive a dc transformer mod a winding resistance of R _L . Ig	lel of a non-ideal Buck converter with an indu gnore all other sources of losses.	ctor having (03	3)	
1B.	It is desired that the non-ideal buck converter (with inductor resistance R_L) operates with at least 70% efficiency when the input voltage is 5V and the output is 1V at 1A. Ignore all other losses.				
	(i) At what duty cycle wi	ll the converter operate then?			
	(ii) How large can the ind	luctor winding resistance be?	(02	2)	
1C.	A non-ideal boost converter resistance Ron, and the diode	r has inductor winding resistance R_L , MOSFI e forward voltage drop V_D . All other losses can	ET on state be ignored.	,	
	(i) Derive a dc transform	er model of the converter.			
	(ii) Derive an expression	to find the non-ideal voltage conversion ratio	n Vo/Vs. (05	5)	
2A.	Draw the circuit schematic of voltage Vo. (Apply inductor v	of a SEPIC converter and derive an expression volt sec balance and capacitor charge sec bala	n for output nce.) (02	?)	
2B.	A SEPIC converter has the fo	llowing values			
	Input voltage Vs =48V				
	Output voltage Vo= 12V				
	Switching frequency fs =100	KHz			
	Load resistance R=6 Ω				
	Select values of L ₁ , L ₂ and C ₁ and Δi_{L2} = 25mA (ii) peak vol	such that (i) the input peak current ripple Δ tage ripple on C1, Δv_{c1} is 2% of the dc compo	iL1 = 20mA nent Vc1. (03	3)	
2C.	Draw the circuit schematic c voltage Vo, inductors L_1 and	of a CUK converter and derive the expressions L ₂ , Capacitors C ₁ and C ₂ . (Apply inductor volt-	s for output sec balance	-	
	and capacitor charge sec bala	ance)	(05	5)	
3A.	Design a Flyback converte specifications: Vs= 165V, Vc Determine the (i) turns ratio	er in continuous conduction mode for the p= 15V, Io=5A, fs =100kHz. Specified duty ra (ii) Magnetizing inductance Lm and (iii) Filte	e following itio is 0.42. r capacitor.		
	(Assume current ripple of 40)% and output voltage ripple of 2%.)	(04	I)	

3B.	Calculate the filter inductor and capacitor values for Forward converter operating from a dc input of Vs= 325V, Vo= 10V \pm 0.1V, I ₀ =20A, fs =100kHz. The transistor duty cycle D=0.4. Determine the numerical values of turns ratio N ₃ /N ₁ and N ₂ /N ₁ .	
	(Assume continuous conduction mode and current ripple to be 40% of the average value).	(04)
3C.	Draw the circuit schematic of Full bridge dc dc converter. Also sketch	(01)
	(i) Gate pulses of the switches (ii) inductor voltage and inductor current	(02)
4A.	Make a comparison between the isolated topologies of the dc dc converter	(03)
4B.	A Series resonant Half bridge dc dc converter has the following specifications: dc input of Vs=550V, Lr=30 μ H, Cr=0.3 μ F, Ro=8 Ω . The switching frequency fs= 150kHz. Determine output voltage V ₀ .	(03)
4C.	Draw the circuit schematic of a Parallel resonant Half bridge dc dc converter. Sketch the waveforms of the inductor current and capacitor voltage in the tank circuit for discontinuous conduction mode. Show the devices conducting current for each subinterval. Also mention the type of switching for all the four devices.	(04)
5A.	A buck converter is realized using a half wave ZCS switch. With a circuit schematic, sketch the waveforms of inductor current i_{Lr} and Capacitor voltage v_{Cr} . Clearly mark the four modes of operation. Also mention the switches conducting in each mode.	(03)
5B.	A half wave ZVS buck converter has the following data: Vs= 20V, fs=360kHz. Mode 1 operates for 0.2 μ s. Mode 4 operates for 1.45 μ s. Determine the output voltage of the converter. Also sketch i _{Lr} and v _{Cr} .	(02)
5C.	Obtain the state equation of the small signal model of a Buck converter using state space averaging technique	(05)