Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER B.TECH. (E & C) DEGREE END SEMESTER EXAMINATION
DECEMBER 2018
SUBJECT: ADVANCED EMBEDDED SYSTEM DESIGN (ECE - 4001)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. (a). What is the role of PSoC5 on CY8CKIT-044?
(b). What is the use of CY_ISR and CY_ISR_PROTO macros of PSoC creator?
(c). What is the difference between isr_Start( ) and isr_StartEx( ) API routines of PSoC Creator?
(d). What is the PSoC creator's API routine to bring CPU back to bootloader from bootloadable?

1B. Write the format of following ARM Cortex-M0 registers and explain the significance of each bit/register. (a). PSR (b). PRIMASK (c). CONTROL (d). r13 (e). r14

1C. List any eight features of PSoC4200M and explain the dynamic reconfiguration of PSoC.

(4+3+3)

2A. (a). For PSoC4200M, Define C Programming Macros
i. To configure GPIO pin into any of the drive mode
ii. To write into a GPIO pin
iii. To read from the GPIO pin
While configuring macros, use PSoC register names given as in **Table 2A.**
(b). Explain the significance of "volatile" keyword in defining C programming macros.

2B. What is Bootloader? Explain its function flow using flowchart.

2C. With neat state diagram, explain processor modes, states and stack pointer selection in ARM Cortex-M0 processor.

(4+3+3)

3A. (a). Assume just before occurring an exception, the CPU is in thread mode and using PSP as an active stack pointer. If an IRQ1 exception occurs then what will be the LR value immediately after entering into ISR?
(b). Just before occurring an IRQ2 interrupt, if xPSR=0x01000000 & SP=0x20007FEC then what will be the xPSR immediately after entering into IRQ2's ISR?
(c). Assume the CPU is in ISR and the contents of stack memory is as shown in **Fig. 3A.** Now, if CPU executes BX LR instruction then what will be the content in Stack Pointer?
(d). Assume the CPU is in ISR and the contents of stack memory is as shown in **Fig. 3A**.

Now, if CPU executes BX <0xFFFFFFF9> instruction then what will be the destination address into which CPU will return?

3B. Write an algorithm that need to be followed to configure IMO frequency in PSoC 4200M.

3C. List the range of software components present inside an ARM based CPU's program image. In PSoC, what are the CPU functions to be executed as part of its boot sequence? Explain briefly the operation of each function.

(4+3+3)

4A. Draw the internal block diagram of PSoC 4200M's Watch Dog Timer. Write the steps to configure it as a periodic interrupt generator.

4B. With neat flow chart, explain the ARM Cortex-M0 exception exit sequence.

4C. The schematic in *.cysch* file of PSoC Creator is as shown in **Fig. 4C**. Write C code to convert analog input to digital and send the result to PC using UART.

(4+3+3)

5A. List all the power saving modes of PSoC and write the status of CPU, SRAM, UDBs, GPIOs in each mode. With transition diagram, explain how to enter into each power mode along with their wakeup sources.

5B. Draw the PSoC's UDB block diagram. Explain the configuration of Instruction, Registers, Input and Output windows of DP element of PSoC creator's UDB editor while implementing the Up/Down counter's state diagram shown in **Fig. 5B.**

(5+5)

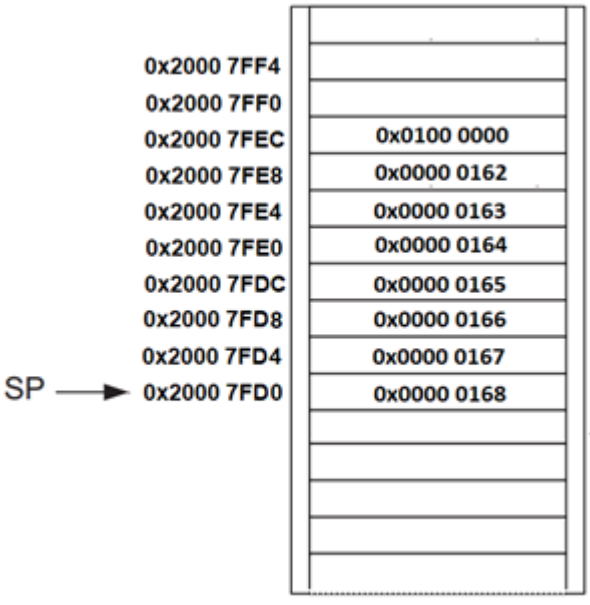

Fig. 3A

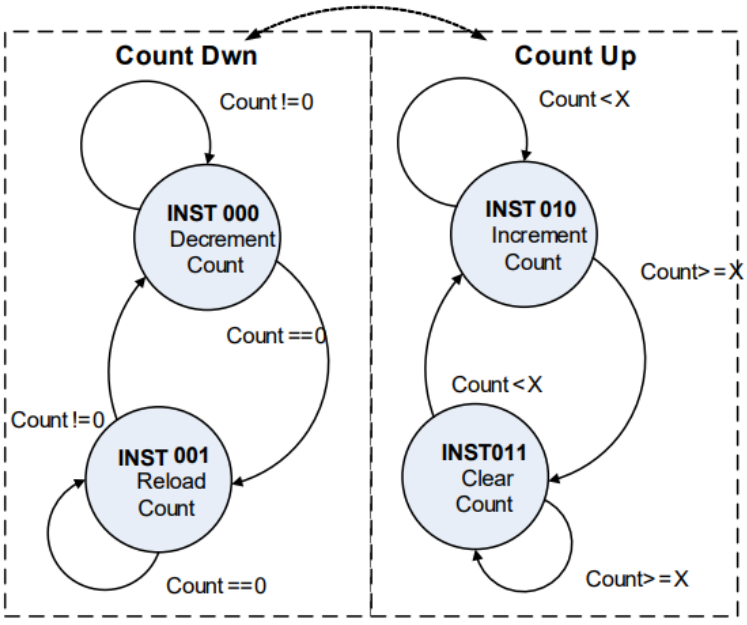

Fig. 5B

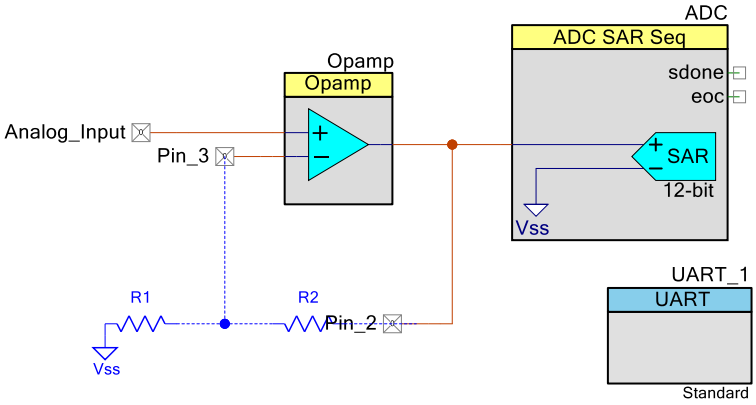

Fig. 4C

Table. 2A

Register	PSoC Naming convention
IO Port Data register	GPIO_PRTx_DR
IO Port Iin State	GPIO_PRTx_PS
IO Port Configuration	GPIO_PRTx_PC

x is port number