Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER B.TECH. (E & C) DEGREE END SEMESTER EXAMINATION
DECEMBER 2018/JANUARY 2019
SUBJECT: ADVANCED EMBEDDED SYSTEM DESIGN (ECE - 4001)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Assume the features of an embedded system are given in the form of technical tasks *T0, T1, T2, T3, T4* and *T5*. The flow of execution of these tasks is shown in **Figure 1A**. The execution time(T) and power consumption(P) of each task by various processing elements is given in **Table 1A**.

i. Explain the concept of co-synthesis in a typical embedded system design flow.

ii. Find suitable application mapping to design the system with power consumption less than 30 mWatts by drawing activity scheduling graph.

iii. Find suitable application mapping to design the system with total processing time less than 20msec by drawing activity scheduling graph.

1B. With the help of transition diagram, explain the power saving modes of PSoC 4.

5+5

2A. Define a C function for PSoC4200M that can be used

(a). just before entering into critical section of the code.

(b). to set ISR address in vector table for IRQ0 to IRQ31.

(c). to set the priority for exceptions IRQ0 to IRQ31.

(d). at the exit of critical section of the code.

2B. Write the special features those Digital signal processor should have over other data processing elements.

2C. Draw the block diagram of PSoC 4200M's clocking system and explain each block.

4+3+3

3A. In ARM Cortex-M0, While CPU is executing the main program, assume the content of CPU registers is as shown in **Table 3A** Now if IRQ3 interrupt occurs, what will be the content in below registers immediately after entering into the corresponding interrupt handler?

i. LR ii. xPSR iii. SP iv. Content in 0x20003FD4 addressed location

3B. In context of PSoC 4 interrupts, explain the use of following

i. **<*instance_name*>_Start()** and **<*instance_name*>_StartEx()** API routines

ii. **CyEnterCriticalSection()** API routine

iii. **Bootoadable_Load()** API routine

3C. Assume the schematic in ***.Cysch*** file of PSoC creator is as shown in **Figure 3C**. ***Pin_Start_Bootloader*** is configured to **Resistive Pull Up** mode with **Falling edge** interrupt and connected to P0[7] of CY8CKIT-044. ***Pin_LED*** is configured in **strong drive mode**. Bootloadable is linked to a Bootloader, which is configured to communicate with Host using I2C. Rest all are default.

Fill ***main.c*** file of PSoC Creator with appropriate code to do the following:

CPU should toggle ***Pin_LED*** continuously (with a period of 1 sec) as long as the switch on CY8CKIT-044 is not pressed. When switch pressed, CPU Should start executing Bootloader and it should remain doing the same until HOST update flash with new application.

4+3+3

4A. With neat diagram, explain briefly the drive modes of PSoC 4200M GPIOs

4B. Write steps to configure PSoC 4200M's watch dog timer for periodic interrupt generation

4C. Write the default API routines of PSoC creator to

(a). generate delay in milliseconds (b). drive processor into hibernate mode

(c). find the reset reason (d). unfreeze GPIO pins

(e). enable global interrupts (f). set IMO frequency

4+3+3

5A. Assume the schematic in *.cysch* file of PSoC Creator is as shown in **Figure 5A.**

i. Choose values of R1 and R2 to give an opamp gain of 11

ii. Write C code to convert analog input to digital and send the result to PC using UART.

5B. Draw the block diagram of PSoC4 UDB and explain the advantage of data-path availability in it. List out the methods available to embed functionality into PLDs and Datapath of PSoC UDBs.

5C. Explain the configuration of Instruction, Registers, Input and Output windows of DP element of PSoC Creator's UDB Editor while implementing the state diagram shown in **Fig.5.C**.

4+3+3

Table 1A

	GPP		DSP		FPGA		ASIC	
Task	***T(ms)***	***P(mw)***	***T(ms)***	***P(mw)***	***T(ms)***	***P(mw)***	***T(ms)***	***P(mw)***
T0	24.6	2.1	8.4	9.4	3.2	17.2	1.8	26.2
T1	7.2	9.7	9.7	7.2	17.6	2.8	14.8	7.0
T2	6.4	16.4	7.0	14.8	26.4	1.2	22.7	2.2
T3	26.2	1.8	18.4	2.4	9.4	8.4	8.8	8.8
T4	16.4	6.4	17.2	3.2	2.2	22.7	2.1	24.6
T5	6.4	16.4	1.2	26.4	2.8	17.6	2.4	18.4

T(ms)*-Time taken by each task to execute(in milli seconds).*

P(mw)*- Power consuming by each task (in milli Watts).*

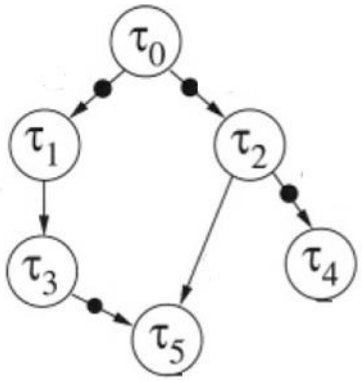

Figure 1A

Table 3A

R0=0x00000000	R1=0x000000C0	R2=0xE000E100
R3=0x00000001	R12=0xE000E400	LR=0x000001F1
PC=0x000001F0	xPSR=0x01000000	SP=MSP=0x20003FE4

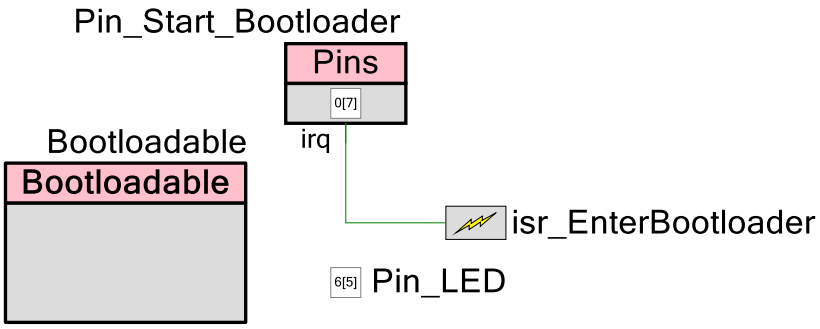

Figure 3C

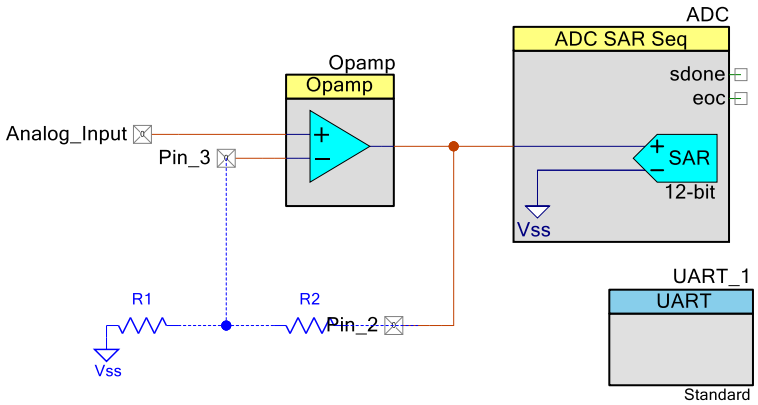

Figure 5A

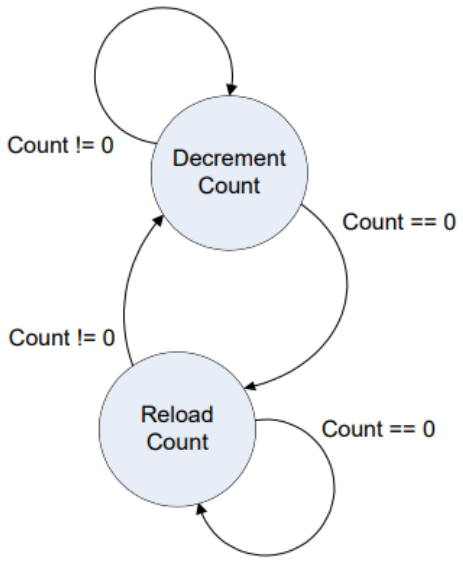

Figure 5C