Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER B.TECH. (E & C) DEGREE END SEMESTER EXAMINATION
DECEMBER 2018/JANUARY 2019
SUBJECT: ANALOG AND MIXED SIGNAL DESIGN (ECE - 4013)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Design the 4th order 455 kHz unity gain Butterworth LPF with normalized transfer function given by

$$H_d(s) = \frac{1}{s^4 + 2.613s^3 + 3.414s^2 + 2.813s + 1}$$

use equal transconducatnce approach and assume g_m=30.1 µS. Draw the circuit diagram and mention the advantages and disadvantages of 4th order LPF with unity feedback gain.

1B. Draw the circuit diagram of triple cascode current mirror and derive the expression for output resistance. Consider the triple cascode current sink, assume all transistors operating in saturation region with I_d=10 µA, V_{DS}=50V, amplification factor gmr0=50. Find the value of output resistance. Neglect the bulk effect

(5+5)

2A. With neat diagram explain mixed signal layout strategy used to improve the performance of analog circuitry.

2B. With neat diagram explain first order sigma delta modulator and implement using switched capacitor technique. State how the resolution of ADC can be enhanced without using an external ADC.

(5+5)

3A. Consider a 1:8 current sink circuit, assume that the lengths are identical. Find the ratio error, if W1 is (5± 0.05) µm and W2 is (40±0.05) µm. Find the ratio error if this current amplifier with ΔW correction, by considering 8 MOSFETs in parallel.

3B. Consider a 2 integrator loop distributive feedback with one feedback factor and show all the possible biquad transfer function.

(3+7)

4A. Draw the circuit of parasitic insensitive integrator using switched capacitor technique and derive the expression for transfer function.

4B. Using switched capacitor technique implement the passive RC first order low pass filter so that product of RC is 1msec and 3-dB frequency is 159Hz.

4C. With neat diagram explain compensation of finite bandwidth effects in Operational Trans conductance Amplifiers.

(4+3+3)

5A. The differential amplifier shown in Figure 5A should achieve a differential gain of 40 with a power consumption of 2mW. All the transistors operate with the same V_{OV}. Find (W/L) of all transistors, V_{g3}, V_{G4}, V_{G5}. Assume $\mu_n C_{ox} = 400\ \mu A/V^2$, $\mu_p C_{ox} = 100 \mu A/V^2$, $\lambda_n = 0.1/V$, $\lambda_p = 0.2/V$ and $V_{tn} = |V_{tp}| = 0.4V$

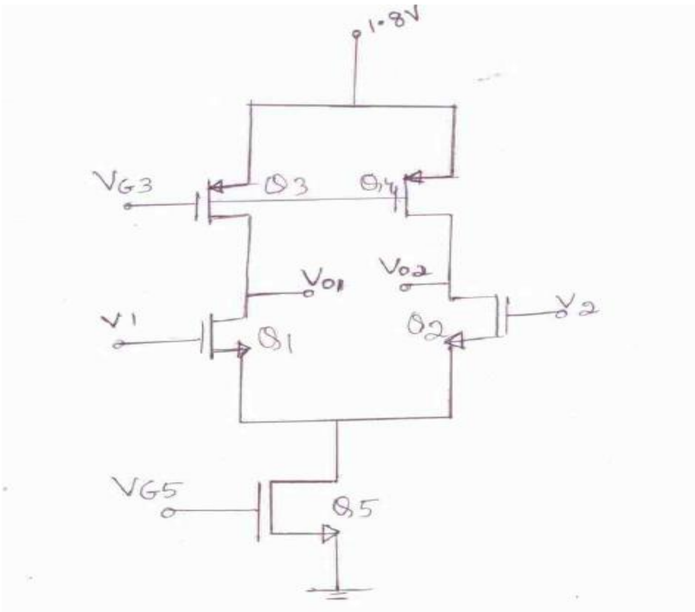

Figure 5A

5B. Give Operational Trans conductance Amplifier implementation of lossy integrator in differential mode and derive the transfer function.

(5+5)