Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER B.TECH. (E & C) DEGREE END SEMESTER EXAMINATION
DECEMBER 2018/JANUARY 2019
SUBJECT: LOW POWER VLSI DESIGN (ECE - 4014)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Discuss the design issues related to supply gating technique for leakage power reduction using suitable circuits. Also explain the merits and demerits of supply gating technique.

1B. Explain i) Stacking of transistors and ii) LECTOR technique for low power operation.

(5+5)

2A. Describe dual V_{dd} technique with its salient features for reducing dynamic power in CMOS circuits.

2B. Explain implementation of differential signalling for power reduction in VLSI circuits and list it's advantages and disadvantages.

(5+5)

3A. Explain i) bus segmentation technique and ii) bus invert encoding techniques for reducing bus power in VLSI circuits.

3B. With the help of suitable illustration discuss i) input ordering and ii) logic restructuring for reducing switching activity.

(5+5)

4A. Discuss various sources of leakage current in MOSFETs and briefly explain ONE technique each for reducing such leakage current.

4B. Discuss the need and impact of using repeaters in interconnects.

(5+5)

5A. List and discuss dynamic power management policies and compare them.

5B. With suitable examples explain i) procrastination scheduling and ii) loop unrolling technique for low power designs.

(5+5)