Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER B.TECH. (E & C) DEGREE END SEMESTER EXAMINATION
NOVEMBER 2018
SUBJECT: LOW POWER VLSI DESIGN (ECE - 4014)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Discuss the hierarchy of low power design and its significance from the point of view of power savings and speed.

1B. With the help of neat diagram describe dynamic supply gating technique and show how it can be extended to random or arbitrary logic. List the key benefits of the technique.

(5+5)

2A. Explain dual V_{DD} technique for leakage reduction in CMOS circuits and compare it with VTCMOS technique.

2B. Explain i) Device stacking and ii) Gate length biasing for reducing leakage power in CMOS circuits. (5+5)

3A. Discuss the sources and impact of crosstalk in buses and suggest remedies.

3B. For a CMOS inverter a clock signal is fed at its input with rise and fall times are equal to 1ns. Assume that k'n =80 $\mu A/V^2$, operating frequency of 100MHz.

(i). Find the average short circuit power dissipated. Assume that the short circuit current waveform is triangular, and flows for the entire duration of tr and tf.

(ii). Repeat the problem if tr = 1.5 ns and tf = 1.0.ns

(W_P/L_P = 4/0.5 and W_N/L_N = 2/0.5, V_{DD} = 3.3V, μ_P = 230 cm^2/V-Sec, μ_N = 545cm^2/V-Sec, Vtn = 0.8V, Vtp = -0.8V)

3C. Why latch based clock gating is preferred? Give reasons.

(4+3+3)

4A. Explain the significance of Just-in-Time processing in the context of low power processing and discuss the techniques employed to achieve Just-in-Time processing.

4B. Calculate the switching activity at each node in a half adder circuit built using two input NAND gates. Assume that both inputs A and B have a switching probability of 0.5.

4C. Discuss the motivation for low swing buses and list its merits and demerits.

(4+3+3)

5A. Describe: i)Object code compression and ii)procrastination scheduling for system level power reduction.

5B. Discuss the merits and demerits of predictive policy for dynamic power management.

5C. With the help of suitable analysis and expressions, illustrate the basic principle of adiabatic switching.

(4+3+3)