Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER B.TECH. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER EXAMINATIONS, DECEMBER – 2018

SUBJECT: REAL TIME EMBEDDED SYSTEMS [ICE 4003]

Time: 3 Hours **MAX. MARKS: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Explain the basic model of real time systems with block diagram. **(3)**

1B. Classify real time tasks with examples for each. **(3)**

1C. Consider 6 processes P_1, P_2, P_3, P_4, P_5 and P_6 arriving in ready queue at time 5, 4, 3, 1, 2 and 6 respectively. If the burst time requirements are 5, 6, 7, 9, 2 and 3 respectively. Use Round Robin scheduling method to find the average waiting time, average turn around time and response time. Assume higher values indicate higher priorities and Quantum Time = 3. **(4)**

2A. Explain Foreground background scheduler. Consider a Real Time system in which the tasks are scheduled using Foreground Background scheduler. There is only one periodic foreground task T_i = ($e_i = 50ms,\ p_i = 100ms, \Phi_i = 0, d_i = 100ms$) and the background task T_b = ($e_b = 1000ms$). Suppose an overhead of 1ms on account of every context switch is to be taken into account, compute the completion time of T_b. **(5)**

2B. A cyclic scheduler is to be used to run the following set of periodic tasks on a processor: T_1 = ($e_1 = 1,\ p_1 = 4$), T_2 = ($e_2 = 1,\ p_2 = 5$), T_3 = ($e_3 = 1,\ p_3 = 20$), T_4 = ($e_4 = 2,\ p_4 = 20$). Select an appropriate frame size. **(2)**

2C. Compute the different types of inversions that each task might have to undergo for the task graph shown in **Fig.2C**. Assume tasks have been sorted in order of priority. Task T_1 has highest priority and task T_6 has least priority. **(3)**

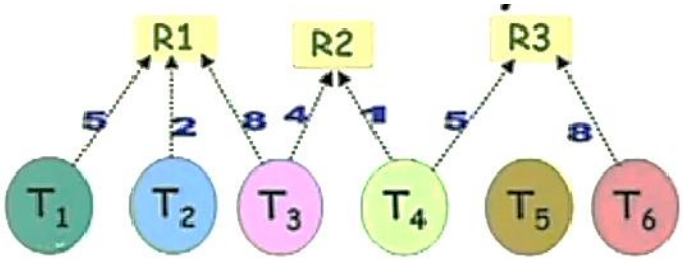

Fig.2C

3A.	Compare centralized clock synchronization and distributed clock synchronization schemes with relevant figures.	**(4)**
3B.	Explain Deadlock and chain blocking conditions with suitable examples.	**(4)**
3C.	List any two causes of failures in the hardware design.	**(2)**
4A.	Describe static pairing and N modular redundancy with relevant figures.	**(4)**
4B.	Explain RETHER protocol.	**(4)**
4C.	List the disadvantages of assembly language based development.	**(2)**
5A.	Explain host target and preemption point approach in Operating systems.	**(4)**
5B.	Write a short note on VxWorks and QNX operating system.	**(4)**
5C.	Define Task preemption time and static priority level.	**(2)**

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