Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER B. TECH. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER DEGREE EXAMINATIONS, DECEMBER – 2018

SUBJECT: VLSI DESIGN [ICE 4004]

TIME: 3 HOURS **MAX. MARKS:50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A Compare between CMOS and bipolar technologies. 3

1B Illustrate the p-well process of CMOS fabrication with figures. 4

1C Explain the working of an nMOS inverter with its transfer characteristics. 3

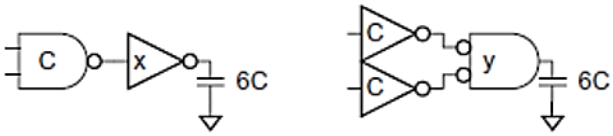
2A An nFET pass transistor has β_n=1.50 mA/V^2 with a process that uses V_{DD}=5 V and V_{Tn}=0.5 V. A logic 1 voltage $V_{in}=V_{DD}$ is applied to the input side, and the output node has a total capacitance of C_{OUT}=84 fF. The output capacitor is initially uncharged. (i) Find the time constant for the logic 1 charging event. (ii) Calculate the rise time in units of picoseconds. (iii) The input is switched to V_{in}=0 V. Calculate the fall time. 3

2B Derive the expression for the mid-point voltage for a 2-input NOR gate. 4

2C A CMOS NOR2 gate is designed using nFETs with a value of βn. The pFETs are both described by βp=2.2βn. Find the value of V_M if V_{DD}=3.3 V, V_{Tn}=0.65 V and V_{Tp}=-0.8 V. 3

3A Draw the RC equivalent circuit for a 2-input XOR gate. 4

3B Calculate the path effort for the following circuits: 3



3C Briefly explain the different structured design techniques. 3

4A What is the smallest size of ROM that is needed to implement the following: 3
(a) 4-to-1 MUX (b) 3-to-8 decoder (c) 2-bit full adder

4B Find a minimum-row PLA table to implement the following three functions: 4

$$f(A,B,C,D) = \sum m(2,3,5,7,8,9,10,11,13,15)$$

$$g(A,B,C,D) = \sum m(2,3,5,6,7,10,11,14,15)$$

$$h(A,B,C,D) = \sum m(6,7,8,9,13,14,15).$$

4C Implement the function $f = a'bc + b'c + ab$ using an FPGA with MUX-based programmable logic blocks 3

5A Briefly explain the different types of FPGA architectures. 3

5B Describe the different types of logical faults encountered in a digital system. 4

5C Explain different elements that yield to the production cost of an integrated circuit. 3

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