Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

SEVENTH SEMESTER B. TECH. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER DEGREE EXAMINATIONS, NOVEMBER - 2018

SUBJECT: VLSI DESIGN [ICE-4004]

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A Explain the working of enhancement mode and depletion mode transistors. 3

1B Illustrate the n-well process of CMOS fabrication with diagrams. 4

1C Describe the working of a CMOS inverter with its regions of operation. 3

2A A pFET pass transistor has an aspect ratio of 8 in a process where K_p = 60 μA/V^2, V_{DD} = 3.3 V and V_{Tp} = -0.8 V. At time t = 0, the output capacitor C_{out} = 50 fF is charged to a voltage of V_{DD} while the input is switched to V_{in} = 0V. (a) Find the fall time at the output node. (b) The input is switched back to V_{DD}. Find the rise time needed to drive the voltage back up to its high value. 3

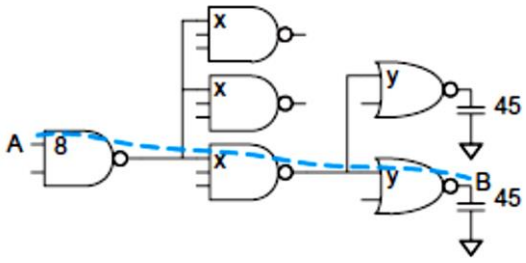
2B Derive the expression for the mid-point voltage for a 2-input NAND gate. 3

2C A CMOS NAND2 is designed using identical nFETs with a value of $\beta_n = 2\beta_p$; the pFETs are the same size. The power supply is chosen to be V_{DD} = 5V, and the device threshold voltages are V_{Tn}=0.6 V and V_{Tp} = -0.7 V. Find the midpoint voltage V_M. What would be the midpoint voltage for an inverter made with the same β specification? 4

3A Sketch the layout of a pseudo-nMOS gate that implements the function: 4

$$f = \overline{A(B + C + D) + E.F.G}$$

3B Estimate the minimum delay of the path from A to B: 3



3C Illustrate the generalized system design flow in implementing an IC with a flowchart. 3

4A The following state table is implemented using a ROM and two D flip-flops (falling edge triggered): 3

Q_1Q_2	$Q_1^+Q_2^+$		Z	
	$X=0$	$X=1$	$X=0$	$X=1$
00	01	10	0	1
01	10	00	1	1
10	00	01	1	0

Draw the block diagram and the ROM truth table.

4B Find a minimum-row PLA to implement the following three functions: 4

$$f(A,B,C,D) = \sum m(3,6,7,11,15)$$

$$g(A,B,C,D) = \sum m(1,3,4,7,9,13)$$

$$h(A,B,C,D) = \sum m(4,6,8,10,11,12,14,15)$$

4C Implement the function $f = a'bc + b'c + ab$ using an FPGA with programmable logic blocks consisting of LUT4. 3

5A Classify the different types of ASICs. 3

5B Briefly explain the different types of electrical faults encountered in a digital system. 4

5C Explain the IDDQ testing technique for fabrication defects. 3

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