Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

V SEMESTER B.TECH. (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, DEC/JAN 2018

SUBJECT: FPGA Based Digital System Design [MTE 4014]

REVISED CREDIT SYSTEM

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. Write a Verilog HDL program to design 1024 X16 RAM using Behavioral modeling **(4M)**

1B. Create a user defined primitive (UDP) for a SR flip-flop. **(3M)**

1C. Write a Verilog HDL program to implement the OR gate using switch level modeling **(3M)**

2A. Write a Verilog HDL code to design parallel adder cum subtractor using Full adder as sub module and Half adder as Leaf cell in gate level modeling. **(4M)**

2B. Generate the list of faults that can be detected for the logic diagram shown in **fig.Q 2(B)** by test vector {11} using parallel fault simulation with a machine word length W=3. **(3M)**

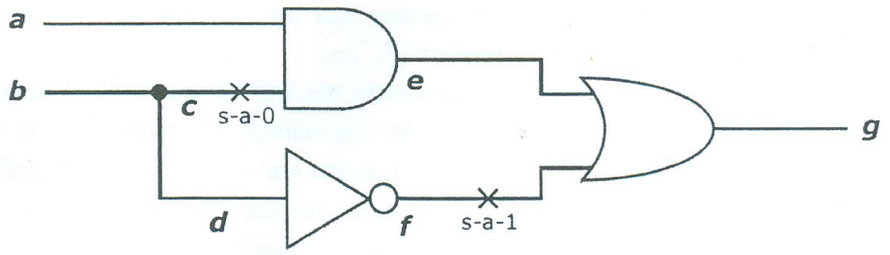

fig.2Q (B)

2C. Design 3:8 Decoder using PLA **(3M)**

3A. Implement the following functions in appropriate PROM **(4M)**

F1 = A B C

F2 = A + B + C

F3 = A' B' C'

F4 = A' + B' + C'

F5 = A xor B xor C

F6 = A xnor B xnor C

3B. Write a Verilog HDL program to implement BCD to Gray code converter using if-else statement. **(3M)**

3C. Generate the list of faults that can be detected for the logic diagram shown in **fig.3Q (C)** by test vector 10010 using deductive fault simulation. **(3M)**

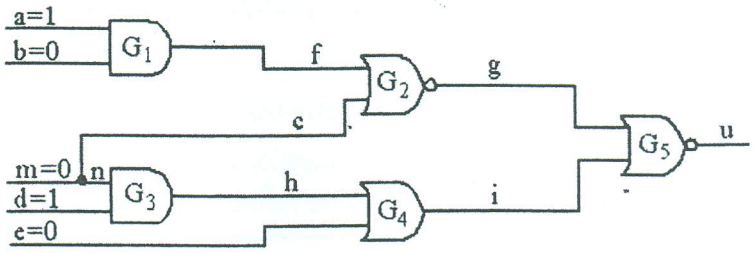

fig.3Q (C)

4A. Design 2-bit comparator using XILINX XC3000 series CLBs. **(4M)**

4B. Write a Verilog HDL program to BCD adder in dataflow modeling **(3M)**

4C. Design SR LATCH using ACTEL FPGA ACT- 1 series Logic module **(3M)**

5A. The ABC Saw Mill is the smallest Canadian producer of fire wood. They wish to automate their log-cutting efforts and have decided to design the conveyor belt system shown in **fig.5Q (A).** You have been commissioned to develop the synchronous sequential saw controller that can detect the length of wood logs and cut only the logs that are long. For simplicity, you may assume that all logs are of only two sizes, either LONG or SHORT. Using two sensors (S_1 and S_2), the SHORT logs will never pass under both sensors at the same time, however, the LONG logs will. The sensor input will be set to logic high when a log is under the sensor, otherwise the input it will remain at zero. After a LONG log is detected (i.e. the end of the log passes sensor S_2), the SAW output must be asserted, which will pause the conveyor belt and lower the saw to cut the log. You may also assume that there will always be sufficient space between logs such that two logs will never be under the sensors at the same time. **(5M)**

For all input sequences that are not physically possible, ensure that your system returns to the "initial" state. Furthermore, all unused states should return your system to the "initial" state. Draw a Mealy model state diagram and write Verilog code to implement above design on FPGA.

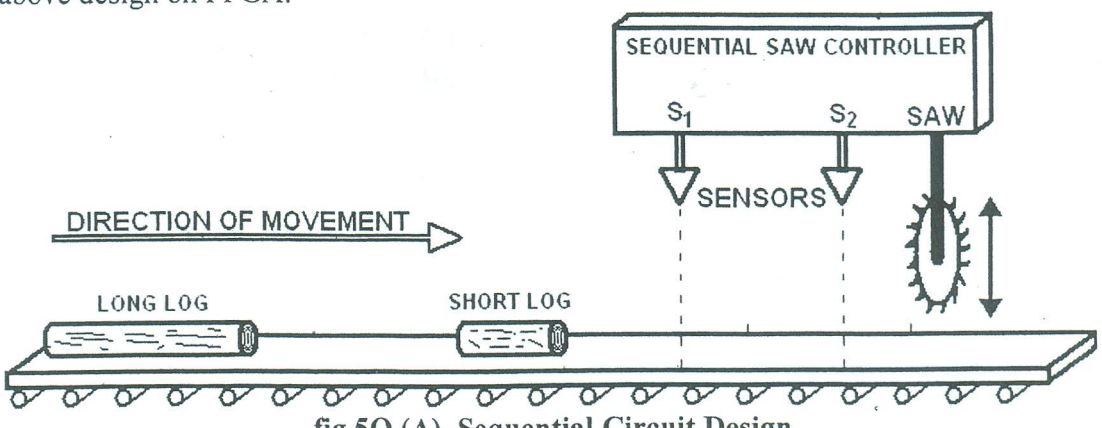

fig.5Q (A) Sequential Circuit Design

5B. For the circuit depicted in the **fig.Q5(B)** use the Boolean difference method to generate all the tests (that is, combination of input variable values) for "Line-a" at s-a-0 **(5M)**

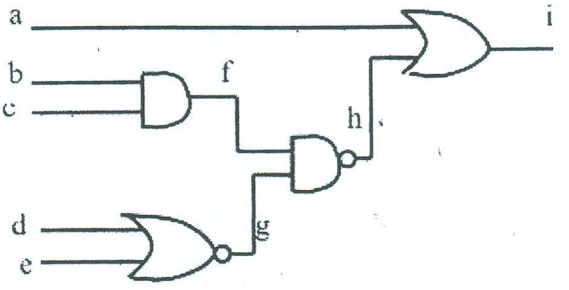

fig.Q5(B)