Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

V SEMESTER B.TECH. (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2018

SUBJECT: FPGA Based Digital System Design [MTE 4014]

REVISED CREDIT SYSTEM
(30/11/2018)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. Write a Verilog HDL code to generate 6.25MHz from 100MHz input using suitable no.of 4-bit ring counters in Behavioral modeling **(4M)**

1B. Create a user defined primitive (UDP) for a JK flip-flop. **(3M)**

1C. Write a Verilog HDL program to implement the following function using switch level modeling $Y = \bar{A}\bar{B} + \bar{C}$ **(3M)**

2A. Write a Verilog HDL program to implement (i) 8-bit First in-First out (FIFO) register reading operation (ii) 8-bit Last in-First out(LIFO) register reading operation using behavioral modeling. The working of FIFO and LIFO registers are as shown **fig.2Q (A)** **(4M)**

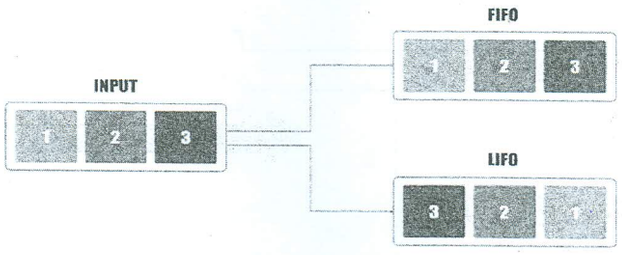

fig.2Q (A)

2B. Generate the possible test vectors for the logic circuit shown in **fig.2Q (B)** using D-algorithm. (**Fault: Line 'g' S-A-0**) **(3M)**

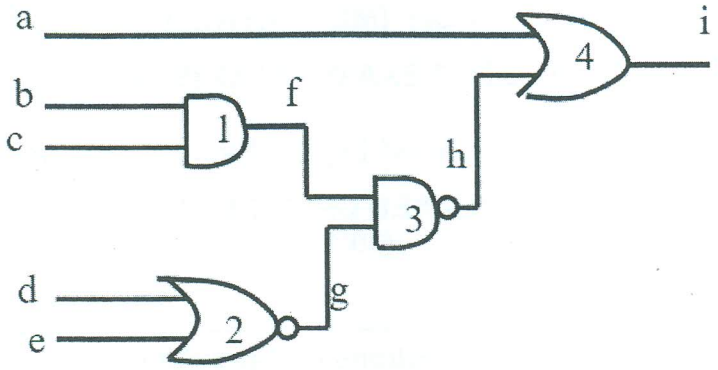

fig.2Q (B)

2C. Implement 2-bit comparator in appropriate PROM **(3M)**

3A. Implement the following Boolean functions using the PAL device **(4M)**

$$W(A, B, C, D) = \sum m(2, 12, 13)$$
$$X(A, B, C, D) = \sum m(7, 8, 9, 10, 11, 12, 13, 14, 15)$$
$$Y(A, B, C, D) = \sum m(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$$
$$Z(A, B, C, D) = \sum m(1, 2, 8, 12, 13)$$

3B. Write a Verilog HDL program to implement BCD to 7 Segment Driver for common anode display using case statement. **(3M)**

3C. Generate the list of faults that can be detected for the logic diagram shown in **fig.3Q (C)** by test vector 010 using deductive fault simulation. **(3M)**

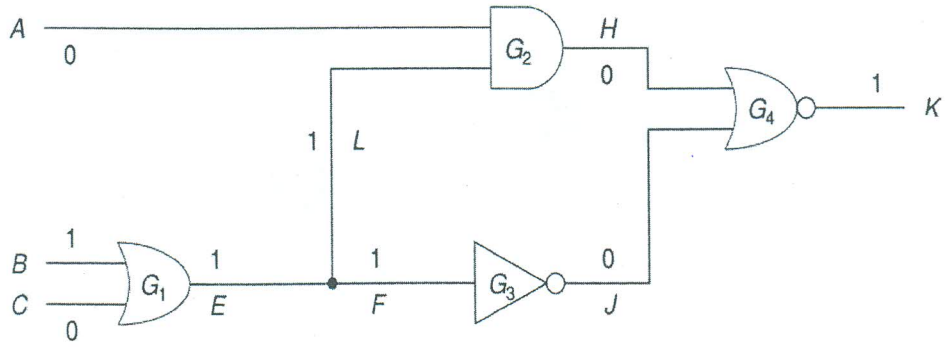

fig.3Q (C)

4A. Design 0101 overlapped sequence detector using XILINX XC3000 series CLBs. **(4M)**

4B. Write a Verilog HDL program to implement 8:3 priority encoder using conditional operator **(3M)**

4C. Design 3-bit Johnson (or twisted) ring counter using ACTEL FPGA ACT- 2 Logic modules **(3M)**

5A. Information bits are encoded on a single line 'X', so as to synchronize with a clock. Bits are encoded so that three or more consecutive 1's or three or more consecutive 0's should never appear on the line X. An error indicating sequential circuit is to be **(5M)**

designed using FPGA to indicate an error by generating '1' on the output line Z, coinciding with the third of every sequence of three zeros or ones. For example, if three or more consecutive ones appear, the output remains one for the third and subsequent clock cycles till bit zero is appeared and vice-versa also. Draw a **Moore** model state diagram and write Verilog code to implement above design on FPGA.

5B. For the circuit depicted in the **fig.Q5(B)** use the Boolean difference method to generate all the tests (that is, combination of input variable values) for X1 **at s-a-0** **(3M)**

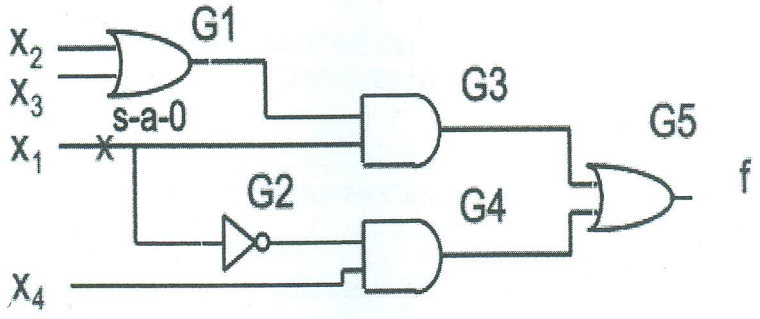

fig.Q5(B)

5C. Generate homing sequence for the state table shown in **Table.Q5(C)** **(2M)**

PS	X=0	X=1
A	B,0	D,0
B	A,0	B,0
C	D,1	A,0
D	D,1	C,0

Table.Q5(C)