Question Paper

Exam Date & Time: 03-May-2019 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
II SEMESTER B.Sc. (APPLIED SCIENCES) IN ENGINEERING END SEMESTER THEORY EXAMINATION-APRIL/MAY 2019
Computer Organization and Architecture [ICS 122]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

1) A) Represent the following numbers in sign and magnitude, 1's complement and 2's complement representations. (6)
   i) -8
   ii) -6

   B) Perform the following operations in 2's complement arithmetic. Take enough number of bits to avoid overflow. (4)
   i) Add +7 and +2
   ii) Subtract +2 from -7
   iii) Add -12 and -10
   iv) Subtract -9 from +17

   C) Write the steps of restoring division method for signed numbers. Divide 4 by -3 using this method. Clearly indicate all the steps. (10)

2) A) Explain the following with respect to memory: (5)
   i) word
   ii) word length
   iii) big endian and little endian assignments
   iv) word alignment.

   B) Write and explain micro operations for fetch cycle by making use of data flow diagram and sequence of events. (5)

   C) With a neat diagram, explain the variable format branch control logic in micro programmed control unit. (10)

3) A) With necessary diagram explain how a virtual address is translated to a physical address. (10)
Consider a virtual address space specified by 24 bits and the main memory space specified by 16 bits. The page number field of the virtual address has 13 bits and the memory is byte addressable. Find
   i) Virtual memory size
   ii) Main memory size
   iii) Number of pages

iv) Size of a page
v) Number of main memory blocks.

B) Explain Direct mapping technique to map main memory address to cache memory. Also explain how the CPU searches for an address in the cache in this mapping technique. (4)

C) Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte block size and 20-bit address. Determine the size of main memory and cache memory. Show the main memory address format if the mapping technique used is (6)
i) Direct mapping
ii) 4 way set associative mapping.

4) A) Explain Booths algorithm for 2's complement multiplication with a neat flow chart. Multiply 7 and -6 using this algorithm. Clearly indicate all the steps. (10)

B) Write the number of bits in the different fields of IEEE 32-bit floating point format. Represent +25.625 in this format. (5)

C) Compare Hardwired control unit with Microprogrammed control unit. (5)

5) A) With a neat diagram explain the operation of parallel output interface. (10)

B) Explain clearly the following with respect to cache: (6)
i) Write through and write back policy
ii) Hit, miss and hit ratio
iii) Why do you need replacement algorithm?

C) Write a note on flash memory. (4)

6) A) Explain the asynchronous data transfer over a bus with timing diagram. (10)

B) Write the sequence of events involved in handling an interrupt request from a single device (5)

C) Draw the block diagram of hardware for addition and subtraction of integers and explain its operation (5)

7) A) What is Branch Target Buffer? How it is used for dynamic branch prediction? (10)

B) What is hardware multithreading? Explain coarse grained and fine grained multithreading. (5)

C) Compare CISC with RISC instruction sets (5)

8) A) What is cache coherence? Explain how it is addressed in shared memory multiprocessor system when write back protocol is used. (10)

B) Write the hierarchy list in the hierarchical memory system. How do the size, the cost per bit and the memory access time vary when you go down the hierarchy? (5)

C) Write a note on mesh interconnection network. (5)

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