Question Paper

Exam Date & Time: 11-Jun-2019 (09:30 AM - 12:30 PM)



MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES II SEMESTER B.Sc. (APPLIED SCIENCES) IN ENGINEERING END SEMESTER THEORY EXAMINATION-APRIL/MAY 2019

COMPUTER ORGANISATION AND ARCHITECTURE [ICS 122 - S2]

Marks: 100

Duration: 180 mins.

Answer 5 out of 8 questions.

- Draw the block diagram of a computer with its essential components, showing the connection between processor and memory. List the steps
 A) and to execute the instruction
 - A) needed to execute the instruction

ADD R3, R2, R1

which adds the contents of the registers R1 and R2, stores the result in R3, in terms of transfers between the components shown in your block diagram and some simple control commands. Assume that the address of the memory location containing this instruction is initially in register PC.

- ^{B)} What is sign extension? Explain with an example for both positive and ⁽⁵⁾ negative numbers
- C) Explain the various addressing modes with an example for each (10)
- Write the steps of restoring division method for signed numbers. Divide -4 ⁽¹⁰⁾ by 3 using this method. Clearly indicate all the steps.
- A)

2)

- B) Draw the block diagram and flowchart for unsigned binary multiplication. (10)
 Multiply 12 by 9 using this method. Clearly indicate all the steps.
- ³⁾ Explain Set associative mapping technique to map main memory address to ⁽⁴⁾ cache memory. Also explain how the CPU searches for an address in the cache in this mapping technique.
 - A computer has a memory of 64K words and a cache of 1K words with a block size of 4 words. Determine the number of bits in the main memory address and the cache memory address. Show the main memory address format if the mapping technique used is
 - i) Direct mapping
 - ii) 4 way set associative mapping.
 - C) With necessary diagram explain how a virtual address is translated to a (10) physical address.
 Consider a virtual address space specified by 20 bits. The byte addressable main memory size is 64 kilobytes. If the page number field of

the virtual address is 9 bits, find the following:

- i) Size of the virtual memory
- ii) Number of bits needed to specify the main memory address
- iii) Number of pages
- iv)Size of a page
- v) Number of blocks in the main memory.
- 4) With a neat diagram explain the functioning of microprogrammed control (10) unit
 A)
 - ^{B)} Write and explain micro operations for indirect cycle by making use of data ⁽⁵⁾ flow diagram and sequence of events.
 - C) Explain polling and vectored interrupt methods of handling multiple interrupt ⁽⁵⁾ requests.
- ⁵⁾ Explain the synchronous data transfer over a bus with timing diagram for ⁽¹⁰⁾ one block of data transfer per one bus cycle.
 - A) B)
- A computer has a small associatively mapped data cache capable of ⁽⁶⁾ holding four words. Each cache block consists of one word. When a given program is executed, the processor reads data sequentially from the following addresses: A, B, C, A, D, E, A, D, C, F

i) Assume that the cache is initially empty. Show the contents of the cache for

LRU replacement algorithm and compute the hit rate.

ii) Repeat part (i) for the cache that uses the FIFO replacement algorithm and

compute the hit rate. Indicate clearly all the steps.

- C) Explain clearly the following with respect to magnetic disk memory: (4)
 i) Seek time
 ii) Rotational delay
 - iii) Organization of Data.
- 6) Explain the 4 phases of floating point addition and subtraction. (8) A) B) With a neat diagram explain the operation of parallel input interface. (8) C) (4) Compare synchronous with asynchronous bus. 7) (10)Explain 4 state algorithm for dynamic branch prediction with a neat state diagram. A) B) (5) What is delayed branch? Explain with an example. C) (5) What are the improvements in Microprogrammed control unit over Wilkes design? 8) (10) Explain Snoopy-cache technique for cache coherence. A)

В)	Write a note on ring interconnection network.	(5)
C)	Explain the operation of dynamic memory cell with a neat diagram.	(5)

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