Question Paper

Exam Date & Time: 30-Apr-2019 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
II SEMESTER B.S c (APPLIED SCIENCES) END SEMESTER THEORY EXAMINATION
APRIL / MAY 2019
Logic Design [IEC 121 - S2]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

1)		Using K-map method determine the prime implicate obtain the possible minimal expression for the followingfunction.	(10)
	A)	$F(A,B,C,D) = \Sigma m(8,12,13) + d(1,2,4,6,7,11)$.	
	B)	Distinguish between latch and flip flop. Draw the logic circuit diagram of RS flip flop using NAND gates.	(5)
	C)	Explain reflective property of code. Illustrate with one example.	(5)
2)		Implement the following switching function using a Four input multiplexer $F(A, B, C, D) = \Sigma m (0, 1, 2, 4, 6, 9, 10, 13, 14)$.	(10)
	A)		
	B)	Implement a 5-to-32-line decoder using four 3-to-8-line decoders with enable and one2-to- 4-line decoder.	(10)
3)		Explain what is meant by race around condition in flip-flops? How we solve it.	(6)
	A)		
	B)	List the universal gates? Implement XOR & XNOR gates using universal gates?	(8)
	C)	Design a Full adder using 3:8 Decoder.	(6)
4)		Design mod-6 sequence synchronous counter using D-Flip flop to generate sequence 0,2,3,6,5,1,0	(10)
	A)		
	B)	Using Quine-Mc Cluskey method, obtain minimal expression for the following Booleanfunction $F(A,B,C,D) = \sum m(8,12,13) + \sum \varphi(2,6,9,)$.	(10)
5)		Design a sequence detector for the following sequence "1011" . Show all the required steps. Assume overlapping is allowed.	(10)
	A)		
	B)	Design a 4 bit Up - Down Asynchronous counters.	(10)
6)		Construct and explain a Ring counter for five timing signals .	(8)
	A)		

	B)	Explain difference between PAL and PLA.	(4)
	C)	Write a behavioural VHDL code for 4:1 MUX.	(8)
7)		Design a 4 bit magnitude comparator using basic gates.	(8)
	A)		
	B)	Implement full subtractor using NAND gates only.	(8)
	C)	Perform BCD addition for the following (i) 679.6 + 536.8 (ii) 35 + 13	(4)
8)		Design 16:1 MUX using only 2:1 MUX .	(6)
	A)		
	B)	Explain with logic diagram the operation of 4-bit SIPO unidirectional shift register.	(8)
	C)	Describe with necessary logic diagram how SR Flip Flop can be converted to JK Flip Flop .	(6)

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