Question Paper

Exam Date & Time: 07-May-2019 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTER FOR APPLIED SCIENCES III SEMESTER B.Sc (Applied Sciences) IN ENGINEERING END SEMESTER THEORY EXAMINATIONS APRIL/MAY 2019

ANALOG ELECTRONIC CIRCUITS [IEC 231 - S2]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

1) A) Draw and explain the input and output characteristics of Common Emitter Configuration. Indicate cut-off, saturation and active regions. Give the biasing conditions for all the three regions. (5)

B) Write the expression for α and β of a transistor. A BJT has α= 0.99, $I_B = 25\mu A$ and $I_{CB0} = 200\ nA$. Find a) the DC collector current b) the dc emitter current and c) the percentage error in emitter current when leakage current is neglected. (5)

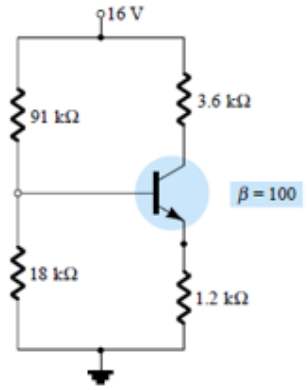
C) Draw the fixed bias circuit. Design a fixed bias circuit using a silicon transistor having β value of 100 , V_{CC}=10V and DC bias condition are V_{CE}=5V and I_C=5mA. (5)

D) Plot the frequency response of RC coupled amplifier and explain how bandwidth is calculated using the response? (5)

2) (5)

A)

Q2A. For the voltage divider circuit using silicon transistor shown in figure Q2A, determine I_B, I_C, V_{CE}, V_C and V_E. What are the advantages of self-bias circuit over fixed bias circuit?



FigQ2A

B) In a multistage amplifier employing 5 stages, with voltage gains of 10, 15, 20, 25 and 30dB.What is the overall voltage gain in dB. If 5mv is applied at the input of this amplifier, calculate the final output voltage (5)

C) An ideal voltage amplifier has infinite input impedance and zero output impedance. Justify this statement with the help of relevant diagram and expressions (5)

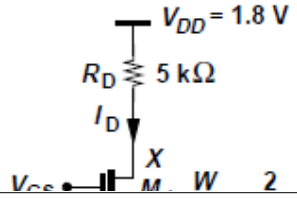
D) An amplifier has a voltage gain of 10, an input resistance of 1KΩ and an output resistance of 10 Ω. The amplifier is connected to a sensor that produces a voltage of 2V and has source resistance of 100Ω and to a load resistance of 50Ω.what will be the output voltage of the amplifier Draw an equivalent circuit of the amplifier, sensor and load. (5)

3) What is base width modulation in BJT? Explain with the help of suitable diagram (5)

A)

B) (5)

Calculate the maximum allowable gate voltage in **Fig. Q3B**, if M_1 must remain Saturated. Assume $\mu_n C_{ox} = 100\ \mu A/V^2$ and $V_{TH} = 0.5V$



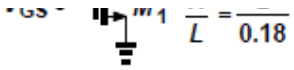


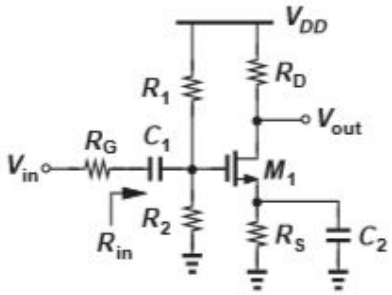
Fig Q3B

C) Compare the common source amplifier with a common emitter amplifier and an emitter follower with a source follower. (5)

D) Construct the high frequency model of a self-bias CS amplifier and obtain the expressions for cutoff frequencies. (5)

4) (10)

A) Design the CS stage of **Fig. Q4A** for a voltage gain of 5, an input impedance of 50KΩ, and a power budget of 5mW.Assume $\mu_n C_{ox}$ = 100 μA/V^2, Vth=0.5V, λ=0 and V_{DD}=1.8V. Also assume a voltage drop of 400mV across Rs.

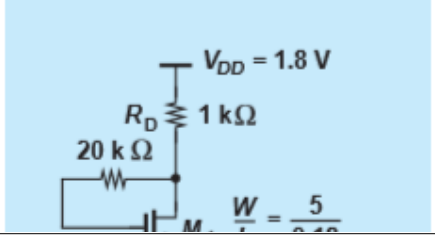


FigQ4A

B) (5)

i) Calculate the drain current of M1 in Fig Q4B if $\mu_n C_{ox}$ = 100 μA/V^2 V_{th} =0.5V and λ= 0. What value of R_D is necessary to reduce I_D by a factor of two?

ii) repeat the above problem if V_{DD} drops to 1.2V. Comment on your answer.



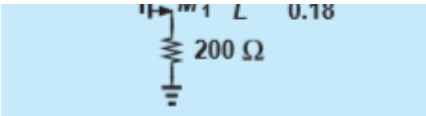


Fig Q4B

C) With neat diagram explain working of n-channel enhancement type MOSFET. Plot ID-VD Characteristics and mark the operating region. (5)

5) (5)

A) Draw the circuit diagram of a Hartley oscillator. Calculate the frequency of oscillations, if L1=0.5 mH, $L2$=1 mH and C_2=0.2 µF. What should be the value of C, if the frequency of oscillations were to be 12 KHz, with other components of the circuit remains same.

B) State and explain Miller theorem. (5)

C) For the circuit shown in **Fig Q5C**, draw the small signal model. Using Miller's theorem, determine Miller's input and output impedances for RF=50Kohms (5)

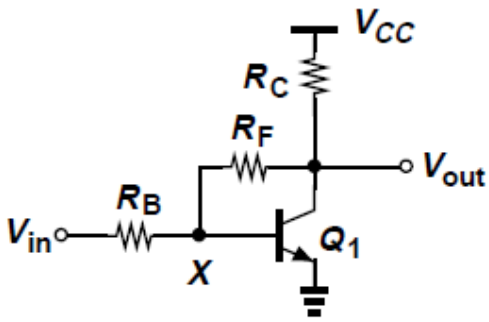


Fig Q5C

D) What is crossover distortion? With the help of suitable diagrams, explain how it can be overcome? (5)

6) A phase shift oscillator using transistor has RL=5.3 KΩ, R=4.6KΩ, C=0.01F.Calculate the frequency of oscillation and also draw the circuit diagram of RC phase shift (5)

A) oscillator.

B) State and explain the Barkhausen criteria for sustained oscillations (5)

C) Derive the expression for voltage gain with feedback for a voltage series amplifier with gain A and feedback factor β. (5)

D) (5)

A low pass filter circuit consisting of a resistor of 47KΩ in series with a capacitor of 47nF is connected across a 10V sinusoidal supply. Calculate the output voltage at a frequency of 100Hz and 10K Hz. Draw the circuit diagram of the filter.

7) Draw the block schematic of i) Voltage shunt ii) Current series feedback amplifiers. What is the effect of series and shunt feedback on the input and output resistance of an amplifier? (5)

A)

B) Explain class A and class B power amplifiers with the help of output characteristic and (5)

load line. Illustrate their operation. What are the theoretical efficiencies of a series-fed class A and class B power amplifiers?

C) Draw the equivalent diagram of crystal and explain its working. Mention any two advantages of Crystal oscillators. (5)

D) The parameters of the equivalent circuit of a crystal are given below: $L = 0.4$ H, $C_S = 0.06$ pF, $R = 5k\Omega$, $C_m = 1.0$pF. Determine the series and parallel resonant frequencies of the crystal. (5)

8) (20)

Explain the following:

i) Sense and return techniques
ii) Negative and positive feedback in amplifiers
iii) Second order effects in MOSFET
iv) Piezoelectric effect

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