Question Paper

Exam Date & Time: 07-May-2019 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
III SEMESTER B.Sc (Applied Sciences) IN ENGINEERING
END SEMESTER THEORY EXAMINATION APRIL / MAY 2019
COMBINATIONAL AND SEQUENTIAL LOGIC [EC 231]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

Missing data, if any, may be suitably assumed

1)	A)	(i) Add 679.6 + 536.8 in BCD number system (ii) Convert the following to the indicated bases (34F.B)16 = (?)$_8$ (84.3)$_{10}$ =(?)$_2$ (iii)Design a combinational circuit for a Full adder using 2 half adders and 1 OR gate	(10)
	B)	Simplify the following Boolean expression and draw the simplified logic circuit AB+(AC)'+AB'C(AB+C)	(5)
	C)	Write a dataflow VHDL code for 4:1 multiplexer	(5)
2)	A)	Simplify the following function using karnaugh map and draw the circuit for the simplified expression using NAND gates. Also determine the essential prime implicant F(A,B,C,D)=∑m(0,4,5,10,11,13,15)	(5)
	B)	Design a combinational circuit to convert 4 bit Binary to Excess 3 code using basic gates.	(5)
	C)	Using Quine Mccluskey method, Obtain the minimal sum for F(A,B,C,D)=∑m(2,3,4,6,9,11,12,13)	(10)
3)	A)	With a neat circuit diagram, explain the working of 4 bit parallel adder/subtractor	(5)
	B)	Implement the following function F(A,B,C,D) = ∑m(0,1,2,3,4,7,8.9,13,15) using (i) 8:1 multiplexer and basic gates (ii) 4:1 multiplexer and basic gates	(5)
	C)	Implement the following multiple output combinational circuit using 4 to 16 decoder with active low outputs. F1=∑m(0,1,2,6) F2=∑m(2,4,6) F3=∑m(0,1,5,6) F4=∑m(0,1,4,7,12,14,15)	(5)
	D)	Write a behavioral VHDL code for 4:1 multiplexer using case statement	(5)

4) Implement the following function using PLA F=∑m(0,2,4,6,7,8,12) (5)

A)

B) Design a circuit for 4 to 2 priority encoder using basic gates (5)

C) Convert (i) SR flipflop to JK flipflop, (ii) T flipflop to SR flipflop (5)

D) Design a Mod 10 ripple up counter using T flipflop (5)

5) Design a synchronous counter using D flipflop that goes through states 0,2,4,6,....The unused states must always go to '0' (000) on the next clock pulse (10)

A)

B) Explain the operation of a master slave JK flipflop with a neat circuit diagram (5)

C) Draw the logic diagram of gated SR latch using NAND gates. Derive the truth table for the same and explain its operation (5)

6) With a neat circuit diagram, explain the operation of 4 bit Universal Shift register (10)

A)

S_1	S_0	Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

B) Reduce the following state table and draw reduced state diagram (5)

Present State	Next State X=0	Next State X=1	Output X=0	Output X=1
A	B	C	1	0
B	F	D	0	0
C	D	E	1	1
D	F	E	0	1
E	A	D	0	0
F	B	C	1	0

C) Write the behavioral VHDL code for 4 bit parallel in serial out shift register (5)

7) Analyze the following synchronous sequential circuit. Draw the logic circuit, excitation table / state table, state diagram, X is the input, A&B are the output (10)

A)

$$J_A=B\ ,\ J_B=X'\ ,\ K_A=X'B\ ,\ K_B=A \text{ xor } X$$

B) Design a Mealy type Sequence detector to detect an overlapping sequence "1010" (10)

8)	A)	Write the structural VHDL code for full adder using 2 half adders and 1 OR gate (Code needs to be written for the entire hierarchy)	(10)
	B)	Explain the operation of 4 bit ring counter with a neat circuit diagram and suitable timing waveforms	(10)

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