Question Paper

Exam Date & Time: 08-May-2019 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTER FOR APPLIED SCIENCES
III SEMESTER B.Sc. (Applied Sciences) IN ENGINEERING END SEMESTER DEGREE EXAMINATION-APRIL/MAY 2019
SWITCHING CIRCUITS AND LOGIC DESIGN [ICS 232]

Marks: 100 **Duration: 180 mins.**

a

Answer 5 out of 8 questions.

1)			Draw the diagram of full adder. Write the truth table for full adder and derive the equations for S_i and C_{i+1}.	(5)
	A)	i		
		ii	Write Verilog code to convert an n-bit gray code into equivalent binary code.	(5)
	B)		Write structural verilog code for 16-bit ripple carry adder constructed using 4-bit ripple carry adders.	(10)
2)			Derive the equations for g_i, p_i, c_{i+1} in carry look-ahead adder. With a neat diagram, explain the construction of 16-bit hierarchical carry look-ahead adder (CLA) using 4-bit CLA with ripple carry between blocks.	(10)
	A)			
	B)		Using tabular method, find the minimum cost SOP expression for the function f(x1,x2,x3,x4)= Σm (0,2,4,5,7,8,9,15).	(10)
3)			Consider the function f(a,b,c,d)= ∑m(0, 4, 5, 6, 9, 10, 11, 15). Use functional decomposition to find the minimal SOP expression for f.	(4)
	A)	i		
		ii	Using k-map, determine the minimum-cost SOP and POS expressions for the function f (x1, x2, x3, x4) = ∑m(4, 6, 8, 10, 11, 12, 15) + D(3, 5, 7, 9).	(6)
	B)		Describe the terms implicant, prime implicant, essential prime implicant and cover.	(4)
		i		
		ii	Consider the function f(x1, x2, x3, x4) = ∑m(0, 2, 4, 5, 10, 11, 13, 15). Using k-map, find the prime implicants, essential prime implicants and minimal cover.	(6)
4)			Explain 4-bit Johnson counter with a neat diagram. Also, tabulate the flip flop outputs and the AND gates required for decoding timing signals.	(8)
	A)			
	B)		Design a 4-bit bi-directional shift register for the following operations using D flip flops and MUXs.	(8)

No change
Arithmetic right shift
Logical left shift
Parallel load

C) Draw the design of 4-bit binary ripple counter. (4)

5) Write Verilog code for 4-bit synchronous down counter designed using T flip flops. (6)

A)

B) Draw the logic diagram of JK flip flop. Write its characteristic table, characteristic equation and excitation table. (6)

C) Design a sequential circuit for a three-bit binary counter. Using T flip flops, draw the logic diagram of the sequential circuit. (8)

6) Write the boolean laws for the following: (8)
i) Distributive. ii) Demorgan. iii) Absorption. iv) Combining.

A)

B) Using algebraic manipulation, simplify the following expressions. (12)
i) A'B+A'B'C'D'+ABCD'
ii) g(a,b,c,d)=a'c'd'+a'bd+bcd+acd'+b'cd'
iii) f= (x1'+x2+x3).(x1'+x2'+x4').(x1'+x3+x4)
iv) f= x2x3'x4+x1x3x4+x1x2'x4

7) A combinational circuit is specified by the following three functions: (4)
F1=X'Y'Z'+XZ F2=XY'Z'+X'Y F3=X'Y'Z+XY

A) i Design a circuit for F1, F2 and F3 using a decoder and other gates.

ii Draw the logic circuit for the following using gates: (6)
a) 4-to-1 MUX. b) 2-to-4 decoder

B) Implement three-input majority function using 4-to-1 MUX. (3)

i

ii Implement three-input XOR function using only, (7)
a) 2-to-1 MUX.
b) 4-to-1 MUX.

8) Discuss the applications of transmission gates with neat diagrams. (6)

A) i

ii Define a tri-state buffer. Write its truth table. (2)

B) Explain the following with a neat diagram. (3)

i CMOS realization of a NOT gate.

ii Explain the following with a neat diagram. (3)
CMOS realization of a NAND gate.

C) Discuss PLA with a neat logic diagram. (6)

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