Question Paper

Exam Date & Time: 02-May-2019 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
IV SEMESTER B.Sc (Applied Sciences) IN ENGINEERING
END SEMESTER THEORY EXAMINATION APRIL / MAY 2019
DSD USING VERILOG [IEC 244 - S2]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

Missing data, if any, may be suitably assumed

1)		Map the function F(a,b,c,d,e)=abc+ab'c+ e'+de using Xilinx XC 3000 FPGA. Determine the number of CLB's and LUT's required. Show the contents in the SRAM cell.	(5)
	A)		
	B)	Implement the following function F=A'B+ABC'+A'B'C using ACT 1 logic module.	(5)
	C)	Explain about semi custom ASIC	(5)
	D)	Implement the given expression F= x1'x3'x4'+x1x2+x3x4 using 4- 2 input LUT's and 1-3 input LUT.	(5)
2)		Implement 3 bit binary to gray code converter using PLA	(10)
	A)		
	B)	Implement the following expression using Altera max FPGA architecture(using shared logic expander) F=A'CD+B'CD+AB+BC'	(5)
	C)	Define Transient fault, logical fault, non-logical fault with an example	(5)
3)		Find the essential test vector and selective test vector for the function F=A'B+C using fault table technique. Consider SA_0 and SA1 fault in all the nodes.	(10)
	A)		
	B)	Implement F=ABC'F+A'CD+B'CD+ABD'F+ABCDE' using ACT2 logic module	(5)
	C)	Find the collapse ratio for the function F=AB+BC using basic gates	(5)
4)		Write a Structural Verilog code for 8:1 multiplexer using 2:1 multiplexer. Write the program for entire hierarchy	(10)
	A)		
	B)	Find the test vector using path sensitization technique for the expression F=	(5)

(A.B)'+(C.D)'. Consider SA_0 fault is at input A node

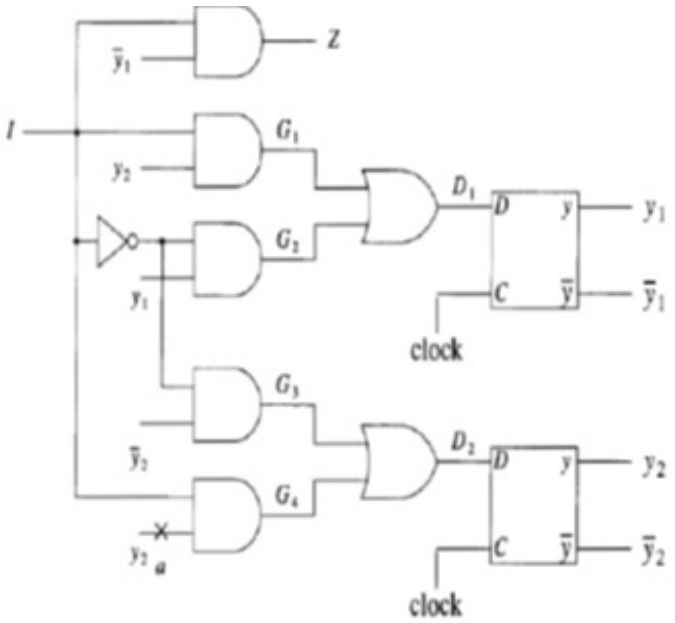
C) Find the test vector for transparent high latch using Iterative test generator. SA_0 fault is at D input not the feedback input (5)

5) Write a sequential Verilog code for 4 bit Ring counter using positive edge triggered clock (10)

A)

B) Write a dataflow Verilog code for 2to 4 decoder with active high enable input (5)

C) Determine the test vector for the sequential circuit shown in Fig.Q5C using ITG (5)



6) Explain ASIC design flow (5)

A)

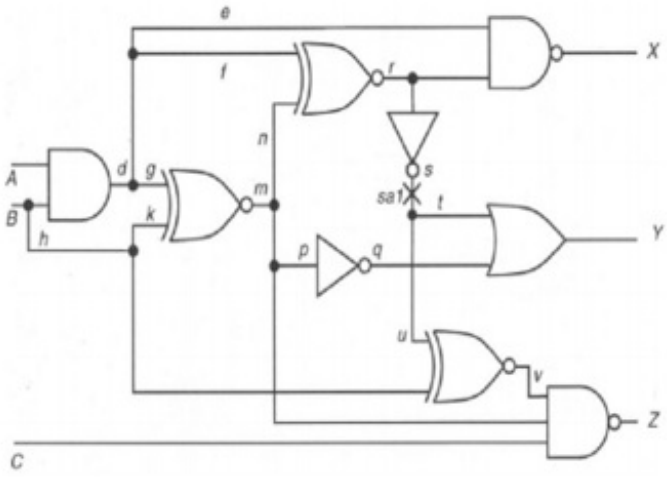
B) Write the behavioral verilog code for 4 bit SISO shift register using if statement (10)

C) Implement the following expression using 3*4*2 PLA (5)
F1(x,y,z)=∑m(0,1,2,4,5) F2(x,y,z)=∑m(1,2,3,4,5)

7) Explain the different types of identifiers used in Verilog HDL (5)

A)

B) Find the test vector using D algorithm for the circuit shown in Fig Q7B. Consider SA1 fault. (10)



C) Map SR latch using Xilinx XC3000 FPGA. Find the number of CLB's and LUT's required. Show the contents in SRAM cell. (5)

8) Write the Structural Verilog code for 4 bit universal shift register. Write the program for (10)

A) entire hierarchy

B) Implement half adder using ACT-1 FPGA series. How many minimum number of logic modules required to implement. (5)

C) Write the behavioral Verilog code for Actel 2 FPGA module using if statement (5)

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