Question Paper

Exam Date & Time: 29-Apr-2019 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTER FOR APPLIED SCIENCES
IV SEMESTER B.Sc. (Applied Sciences) in ENGG. END SEMESTER THEORY EXAMINATION APRIL/MAY 2019
VLSI DESIGN [IEC 243 - S2]

Marks: 100 **Duration: 180 mins.**

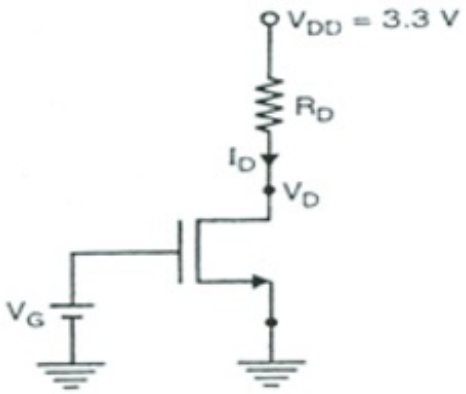
Answer 5 out of 8 questions.

Layout must be drawn using the graph sheet provided.Missing data, if any, may be suitably assumed.

1) A) Derive the relationship between drain to source current I_{ds} and drain to source voltage V_{ds} in resistive and saturation region for an enhancement type NMOS. (10)

B) The MOSFET in **Figure 1B** has V_t= 1V and $\mu_n C_{ox}(W/L)$ = 1 mA/V^2 . Find the drain current and drain voltage for V_G = 2V and R_D = 1kΩ. (10)

Figure 1B



2) A) Define latch-up in CMOS. Why does it occur? What are the remedies for latch- up? Explain in detail with necessary circuit diagrams and curve. (10)

B) Derive the required ratio between Zp.u. and Zp.d. if an NMOS inverter with depletion mode pull up is to be driven from another NMOS inverter with depletion mode pull up (10)

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3) A) With precise figures explain the different steps involved in the fabrication of PMOS transistor. What is the advantage of the self-aligned process? (10)

B) Draw the circuit, stick diagram and layout of two input NAND gate using CMOS design style. (10)

4) A) Explain the working and draw transfer characteristic of NMOS inverter with i) Resistor pull-up ii) Depletion mode transistor pull-up iii) Enhancement mode pull-up (10)

B) Show that the inverter pair delay using two identical pseudo-NMOS inverters is larger by a factor 1.7 than that using minimum size NMOS inverters with depletion-mode pull-up. (10)

5) A) Explain different scaling models. Discuss the effect of different scaling on following parameters:
[i] Gate oxide capacitance C_g [ii] Channel resistance R_{on} [iii] Gate delay T_d (10)

B) Discuss cascaded inverters as drivers for driving large capacitive loads and derive the necessary expressions. (10)

6) A) Given that 1□C_g = 0.01 pF. (10)
i) Find the optimal number of CMOS inverters to be cascaded so as to drive an off-
chip capacitive load of 0.54 pF such that the total delay is minimized.
ii) Give the cascaded structure, clearly showing the L:W ratio.
iii) Show the delay T_d across each inverter stage and hence calculate the overall
delay.

B) An enhancement type NMOS has V_t= 0.8V and $\mu_n C_{ox}$ = 20 μA/V^2 (10)
i)Find (W/L) for V_G=2.8V, V_D=5V, V_S=1V and I_D=0.24mA.
ii) Calculate I_D for V_G=5V, V_D=4V, V_S=2V for same (W/L) as in part (i)

7) A) For CMOS inverter, derive the expression for V_{inv}. Study the effect of $\frac{W_n/L_n}{W_p/L_p}$ on DC transfer characteristics of CMOS inverter and on value of V_{inv}. What is the desired value of V_{inv} and why?.What is Z_{pu}/Z_{pd} ratio for symmetrical CMOS inverter? (10)

B) Give hardware implementation and draw stick diagram for storing following 4-bit words using NMOS ROM structure. word1: 0101; word2: 0010; word3: 1001; word4: 0110 (10)

8) A) Calculate the effective capacitance for the given multi-layer structure in **Figure 8A** for 5μm process. Relative Capacitance value for metal1= 0.075, polysilicon=0.1 and Gate-to-channel = 1.0. (10)

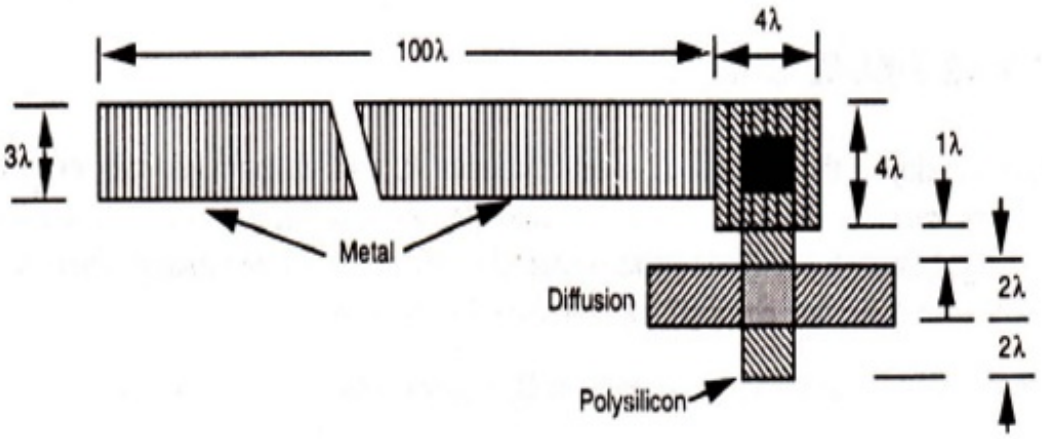

Figure 8A

B) Implement Boolean function $F = \overline{(x+y)\,[z+(w.t)(z+x)]}$ using i) CMOS logic ii) NMOS logic iii) pseudo NMOS logic. (10)

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