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# MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

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**SECOND SEMESTER B.TECH. DEGREE END SEMESTER EXAMINATION**
**APRIL/MAY 2019**
**SUBJECT: BASIC ELECTRONICS (ECE - 1051)**

**TIME: 3 HOURS** **MAX. MARKS: 50**

**Instructions to candidates**

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. For a fixed bias circuit Vcc =12V, $R_B$ =240kΩ, $R_C$ =2.2kΩ, $V_{BE}$ = 0.7V and β = 50
   i) Draw the circuit
   ii) Determine the values of $V_{CE}$, $I_B$ and $I_C$
   iii) Draw the DC load line and locate Q-point

1B. Draw and explain the input and output characteristics of n-p-n transistor in CB configuration indicating the different regions of operation.

1C. Reverse saturation current for a germanium diode at $27^0$ C is 10μA. Calculate the current through it when the applied voltage across it is (i) 0.3V and (ii) -6V.

(4+3+3)

2A. Draw the circuit diagram of an RC coupled amplifier using n-p-n transistor. Mention the role of each component. Sketch the frequency response with and without feedback and indicate the salient features.

2B. A half wave rectifier is supplied with 120V, 50 Hz AC mains through a step down transformer with turns ratio equal to 5:1. Determine the average and RMS value of the load current for a load of 1kΩ and the PIV rating of the diode to be used for proper working. Draw the input and output waveforms.

2C. In the op-amp square wave generator, all resistors are 1kΩ and C = 0.1μF and $\pm V_{SAT}$ = ±12V. Determine the frequency of oscillation of the output signal. Also plot the voltage waveform across the capacitor and the output by marking all the timing and voltage levels.

(4+3+3)

3A. Simplify the following using K-Map and implement using only NAND gates.
F (A, B, C, D) = ∑ m (2, 3, 10, 11, 13, 15) + ∑ d (4, 7, 8, 12, 14)

3B. Realize a 3 bit asynchronous down counter using +ve edge triggered JK flip-flops. Also draw the timing diagram of each flip-flop output.

3C. Draw the logic circuit of 3 bit SISO shift register using D flip flops. Serial data 1010110010 is fed to a 3 bit SISO shift register from LSB. What will be the output of SISO operation after $7^{th}$ clock pulse? How many clock pulses are required to shift the MSB to the output?

(4+3+3)

4A. With a neat block diagram explain the functionalities of each block in a basic communication system.

4B. Derive the time domain expression for AM wave considering single frequency modulating wave from fundamentals and also plot the spectrum for it.

4C. A 360W carrier is simultaneously modulated by two audio waves with percentage modulation of 55 and 65 respectively. Find the modulation index, total power radiated and power in each sideband. Assume RL = 1kΩ.

(4+3+3)

5A. Explain the following pulse modulation schemes with neat waveforms.
i) PAM ii) PWM iii) PPM

5B. For the binary data 101101, Sketch ASK, FSK and PSK Signals.

5C. i) State Nyquist Sampling theorem.
ii) Consider an analog signal $3Cos(50\pi t) + 10Sin(300\pi t) - Cos(100\pi t)$. Determine the minimum sampling rate required to avoid aliasing.

(4+3+3)