Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

(A constituent unit of MAHE, Manipal 576104)

IV SEMESTER B.Tech.(BME) DEGREE MAKEUP EXAMINATIONS JUNE 2019
SUBJECT: DIGITAL SYSTEM DESIGN (BME 2203)
(REVISED CREDIT SYSTEM)
Monday, 17th June 2019: 2 PM to 5 PM.

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to Candidates:

1. **Answer all the questions.**
2. **Draw labeled diagrams wherever necessary.**

1.	(a)	What are fully customized *Application Specific Integrated Circuit* (ASIC)? How it is different than other variety of IC. Explain.	03
	(b)	Design a CMOS NOR gate and explain.	04
	(c)	Identify two benefits of CMOS gate over TTL. Draw a two input NMOS AND gate and indicate ON/OFF state of each transistor for an input "10".	03
2.	(a)	Explain how Programmable Logic Array (PLA) device are different than Programmable Array Logic (PAL) device? Design a full adder circuit using PLA device.	04
	(b)	Design *transmission gate* based multiplexer with buffer stages and explain its operation.	03
	(c)	Given the function $f(w_1, w_2, w_3) = \sum m(0,3,5)$; use Shannon's expansion theorem and expand the function. Identify the co-factors. Draw the 2:1 MUX based circuit with other necessary gates.	03
3.	(a)	Describe the architecture of CPLD (Complex Programmable Logic Device). Explain how it is different from a simple PLD.	04
	(b)	Design a two variable LUT based circuit for FPGA when the given function is $f(W_1, W_2, W_3) = W_3 + W_1 \bar{W}_3 + W_2 W_4$.	03
	(c)	Write a Verilog HDL module for a 4:1 multiplexer.	03

4. (a) What is coarse grained *Field Programmable Gate Array*? Explain how it is different from Mask Programmable Gate Array. 04

(b) Sketch the NMOS AND-OR plane of PLA to indicate the programmed state of the following function: $F = \bar{A}C + \bar{B}$. 03

(c) Explain the following in association with Verilog: 03

(i) **`timescale** 1ns/100 ps

(ii) **always** @ (**posedge** clock)

(iii) **assign** #2 f = A & B;

5. (a) Draw Y- chart and explain its significance. 03

(b) Design a Verilog HDL module for the full adder circuit shown in figure 5(b) using dataflow style. 03

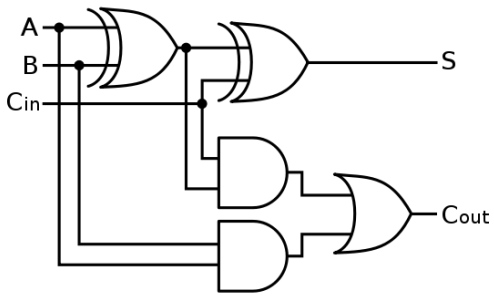

Figure 5 (b)

(c) Design a Verilog module for describing a 4-bit adder using the instance of full adder designed in Q5(b). Draw the digital circuit considered for the design. 04