Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

(A constituent unit of MAHE, Manipal 576104)

IV SEMESTER B.Tech.(BME) DEGREE END SEM EXAMINATIONS APR/MAY 2019
SUBJECT: DIGITAL SYSTEM DESIGN (BME 2203)
(REVISED CREDIT SYSTEM)
Thursday, 2nd May 2019: 2 pm to 5 pm

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to Candidates:

1. **Answer all the questions.**
2. **Draw labeled diagrams wherever necessary.**

1.	(a)	What are Semi-custom types of *Application Specific Integrated Circuit* (ASIC)? Identify the differences in the architecture of channeled and channel less Gate Array ASICs.	03
	(b)	When the digital system design is referred as TOP-DOWN? Explain the method considering an example of N bit adder.	04
	(c)	Design a three input CMOS AND gate. Draw the circuit of the gate and verify the operation.	03
2.	(a)	Design an array multiplier for generating a product "$P_7P_6P_5P_4P_3P_2P_1P_0$" with the help of full-adder and basic gates. Draw the multiplier circuit.	03
	(b)	Write the benefit of a Transmission Gate (TG). Design TG based latch and explain its operation.	04
	(c)	State Shannon's expansion theorem with two variables and decompose the following function using Shannon's theorem with respect to variable B and C. $F(A,B,C) = ABC + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}C.$ Draw the 4:1 MUX circuit with B and C as the select variables.	03
3.	(a)	Describe the typical architecture of FPGA using configurable logic block. Draw the details of configurable logic block and explain.	04
	(b)	Construct a two variable LUT based circuit of FPGA for realization of the given function: $f(W_1, W_2, W_3, W_4) = \bar{W}_1 W_2 + W_1 \bar{W}_3 + W_4$.	03

(c) Write a Verilog HDL code for designing a module that represents a 2 to 4 decoder using dataflow style. Introduce inter-statement delay with time unit of 1ns and precision of 100 ps. 03

4. (a) Draw the circuit of SRAM cell with the NMOS and inverters. Explain the switching operation of the circuit with the help of SRAM cell. 03

(b) Design the NMOS AND-OR plane of a PLA for the programmed condition to realize the function: $f(A, B, C) = BC + A\bar{B} + A$. Draw the diagram and mark the planes. 04

(c) Differentiate a blocking style and non-blocking style of writing Verilog code. Identify a suitable style for cascading the D-FF to formulate them into a 4 bit register. 03

5. (a) Describe the programmable logic block of CPLD and differentiate it from the programmable plane of the PAL. 03

(b) What is instantiation? Design a Verilog HDL module for a 2 variable multiplexer using structural style. 03

(c) Design a Verilog module for describing the circuit shown in Figure 5(c) using the concept of module instantiation. Use the instances of the module designed in Q 5(b) and name the new Verilog module as "*MyLUT*". 04

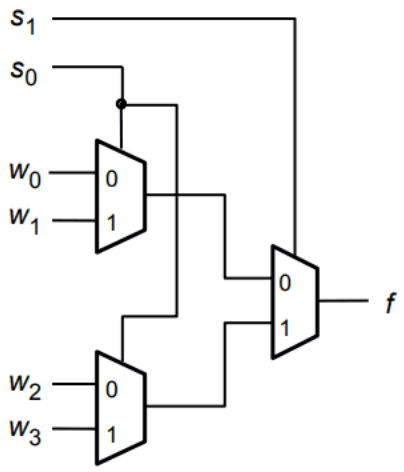

Figure 5(c)