Reg. No.											

MANIPAL INSTITUTE OF TECHNOLOGY

(A constituent unit of MAHE, Manipal 576104)

IV SEMESTER B.Tech (BME) DEGREE MAKE UP EXAMINATIONS, JUNE 2019.

SUBJECT: INTEGRATED CIRCUIT SYSTEMS (BME 2202)
(REVISED CREDIT SYSTEM)
Tuesday, 11th June 2019: 2 PM to 5 PM

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to Candidates:

1. **Answer ALL questions.**
2. **Draw neat labeled diagrams wherever necessary.**

1A)	Draw the circuit of a differential amplifier using Op-Amp. Derive the expression of the output voltage. Under what conditions this circuit can be used as (i) Difference amplifier. (ii) Instrumentation amplifier. Obtain the expressions in both the conditions	3
1B)	Discuss the universal balancing of an Op-Amp.	3
1C)	Derive the expression of total output offset voltage of an Op-Amp. For an inverting Op-Amp amplifier, assume that the amplifier is nulled at 25^0C. If the input is 50 mV dc, calculate the error voltage E_V and output voltage V_O at 40^0C and plot the waveforms. Given input offset voltage drift is 30μV/^{0}C, input offset current drift is 10nA/^{0}C, $R_1 = 100\Omega$, $R_F = 2K\Omega$	4
2A)	Draw the circuit of a logarithmic amplifier with temperature compensation. Derive the expression of the output.	3
2B)	With suitable circuits using Op-Amp, explain the operations of (ii) Active peak detector. (ii) Sample and hold circuit.	4
2C)	Design and draw the circuit of square waveform generator using Op-Amp for the following specifications. Time period is 4 msec. Duty cycle is 75%. Output swing is ±5 Volts.	3
3A)	Derive the expression of $A_V(s)$ of a prototype 2nd order Butterworth active filter.	3
3B)	Design a 4th order Butterworth high pass filter for the following specifications. Lower cutoff frequency is 5 KHz and the overall gain is 20. Also plot the frequency response curve. Given the polynomial is $(s^2 + 0.765s + 1)(s^2 + 1.848s + 1)$	4
3C)	What is delay equalizer and why it is used? Draw the circuit of a delay equalizer.	3

4A)	Draw the internal circuit diagram of 555 timer IC. Explain the functions of each pin of the IC.	3
4B)	Design and draw the circuit of a square wave generator using 555 timer IC for the following specifications. Duty cycle is 20%. Frequency of the waveform is 20 KHz. Output swing is 10 volts. Draw and label the waveforms V_O and V_C.	3
4C)	Design and draw the complete circuit of a regulated power supply using IC 7805 and other components for the following specifications. V_O can be varied between 6 volts to 10 volts. Maximum load current is 250 mA. Input available is 230V/50 Hz AC. Assume 10% ripple factor.	4
5A)	Draw the circuit of a 4 bit R-2R ladder type DAC. Derive the expression of the output. Calculate the values of analog output for all 16 combinations of digital inputs if V_R=6 volts.	4
5B)	With a suitable diagram explain the operation of 3 bit parallel comparator type ADC.	3
5C)	With a suitable block diagram explain the operation of a phase locked loop.	3