Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

IV SEMESTER B.TECH. COMPUTER SCIENCE AND ENGINEERING

END SEMESTER EXAMINATIONS, APRIL 2019

SUBJECT: MICROPROCESSORS [CSE 2203]

REVISED CREDIT SYSTEM
02.05.2019

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL FIVE** questions.
- Missing data may be suitable assumed.

1A. Explain instruction byte queue and pipelining in 8086.State the cases that make the queue slow down the processing. Write the justification for your answer. **3M**

1B. Find the 8086 addressing mode as well as the physical address of the source operand in the following instructions. Assume the values in the registers DS, CS, BX and SI are 9999H, 8888H, 7777H and 6666H respectively. Solve each instruction independently and all answers must be provided in hexadecimal. **3M**

i) ADD AL, 50H[BX]
ii) MOV CL, [BX][SI]
iii) SBB DL, 50H[BX][SI]

1C. Assume A and B are two bytes with values -127 and +127 in the data segment respectively. Write the result in AL register along with the status in SF, CF and OF flags after executing the following set of instructions. **4M**

```
MOV AL, A
SUB AL, B
```

Suppose the values in A and B are swapped and the same set of instructions are executed, what will be the new values in AL, SF, CF and OF?

2A. Write an 8086 assembly language program which works on an array(SRC) of seven characters consisting of alphabets and numbers. The program has to store the following values in a new array (DEST) : 'A' if the character in the SRC list is an alphabet or 'N' if it is a number. Use procedure that passes arguments using pointers to find whether the character is an alphabet or number. Assume the arrays SRC and DEST are defined in the data segment and all the numbers in the array are within the range of 0-9. **3M**

Example: SRC: 5, A, 4, n, R, X, 9
DEST: N, A, N, A, A, A, N

2B. What will be the value in AX register after the execution of each of the code snippets below? Show the internal calculations performed by the processor to execute AAS and DAA instructions with respect to the given code snippets. **3M**

i) MOV AH, 00H
MOV AL, '5'
SUB AL, '9'
AAS

ii) MOV AH, 00H
MOV AL, 99H
ADD AL, 67H
DAA

2C. Assuming the clock frequency of 8086 as 5MHz, calculate the value of "N" in the code snippet below to generate a delay of 2500μs.Show all the necessary calculations. **4M**

	Instructions	**Clock cycles**
	MOV AX, **N**	;4
Loop1:	MOV CX, 10	;4
Loop2:	MOV BX, 0FFH	;4
	DEC BX	;2
	CMP BX, 00h	;4
	LOOPNE Loop2	;18 or 6
	DEC AX	;2
	JNZ Loop1	;16 or 4

3A. i) Draw a neat Interrupt Vector Table(IVT) for the interrupt types *type 32* to *type 36*.Also mention the locations of CS values in IVT corresponding to the types *type 32* and *type 35* respectively. **4M**

ii) Write the values for the following command words when the slave 8259A is connected to IR6 input of master 8259A.Assume IR1,IR3 and IR6 pins of master 8259A are enabled.

a) ICW3 for the master and ICW3 for the slave.

b) OCW1 for the master 8259A.

3B. Write an 8086 assembly language program to perform the following: **3M**

Accept two strings of equal length from the keyboard. The program has to check for matching of characters in the same index in both the input strings and this character wise checking has to be repeated for the entire length of the string. If there is a match, replace that character in the second string by the next character in the first string with wrapping around at the last character. Else, retain the character in the corresponding index in the second string.

Example: Input string1: HELLO Input string2: HULOO Output string: EULOH

3C. i) List the methods of parallel data transfer in 8255A which ensures that the data from the peripheral device is always properly read. **3M**

ii) Write the control words required to initialize the 8255A as follows:

- Set Pins PC0, PC1 and PC2 of Port C.
- Port A and Port C- input ports, port B-output port. Assume 8255A operates in single handshake.

4A. Explain the role of following pins in 8086.Also specify the mode in which each of these pins will be used by 8086. **3M**

i) DT/R' ii)QS1-QS0 iii)ALE

4B. Assume 80286 has to run three programs P1,P3 and P2 in sequence after a system reset. The programs P1 and P2 are to be executed in real mode and P3 to be executed in protected mode. Explain how CPU switches between the modes to complete the execution of programs in given order. Also, write the number of address lines used by 80286 to work in real and protected modes. **2M**

4C. Draw a neat diagram to show how a memory segment in protected mode is addressed by 80386.Assume in paging mode of 80386, a system is set up with one page directory. What should be the values of A31-A22 and A21-A12 bits in the linear address so that **5M**

80386 selects the 901th page frame in 347th page table in the page directory? Show that the maximum physical memory for a CPU with a page directory having base addresses of 1024 page tables is 4GB.

5A. With the help of a neat diagram explain the pipeline stages for integer operation in a Pentium processor. **4M**

5B. Explain any four units of Pentium Pro processor. **2M**

5C. Explain the following features of Pentium4 and Core 2. **4M**
i) Hyper-threading technology ii) 64-bit extension technology