Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FOURTH SEMESTER B.TECH. (E & C) DEGREE END SEMESTER EXAMINATION
JUNE 2019
SUBJECT: DIGITAL SYSTEM DESIGN USING VERILOG (ECE - 2204)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Write a sequential Verilog code using case statement to model 4:1 MUX with data inputs a, b, c, d.

1B. Give the implementation of below given logic function using ACT 2C logic module.

$$Z = B'E + B'D + C'D + BCD'E' + C'E$$

1C. Write switch level Verilog code of 3 input NAND gate build of using PMOS and NMOS switches.

(4+3+3)

2A. Write mixed style Verilog code for implementing a 32-bit ALU that does Addition, Subtraction, Increment and Right rotate.

2B. (a) Find the test vector for the circuit given in **Figure 2B** using Boolean difference method.
(b) Draw the Gajski Y chart and indicate various levels of abstraction in each design domains.

(5+5)

3A. What is deisgn for testability (DFT)? Explain any three techniques for improving the testability of logic circuits.

3B. Write dataflow Verilog HDL code for 4 bit binary to gray converter .

3C. Explain the programmable switching technology used in Xilinx XC 3000 FPGA architecture.

(4+3+3)

4A. Implement $F = AB + \overline{B}C + \overline{C}D + \overline{E}F + \overline{E}G + \overline{E}H + \overline{F}I + \overline{F}J$ using Altera Max 7000 CPLD and sharable logic expander.

4B. Write a sequential Verilog code to model the positive edge triggered D flip-flop with active high reset input.

4C. Give the implementation of 2:4 decoder using ACT 1 logic module(s). The decoder has two inputs namely, A1(MSB), A0 and four outputs denoted by D3(MSB), D2, D1, and D0.

(4+3+3)

5A. Write structural Verilog code for Mod-10 synchronous counter (for the given logic equations). using JK flip flop and required gates as basic building block.

$J_0 = 1$, $K_0 = 1$, $J_1 = \overline{Q_3}Q_0$, $K_1 = Q_0$, $J_2 = \overline{Q_3}Q_1Q_0$, $K_2 = Q_1Q_0$, $J_3 = Q_2Q_1Q_0$, $K_3 = Q_0$

5B. Write structural Verilog code for full adder using 4 to 1 MUX as basic building block.

5C. Write structural Verilog code for ACT 2C logic module.

(4+3+3)

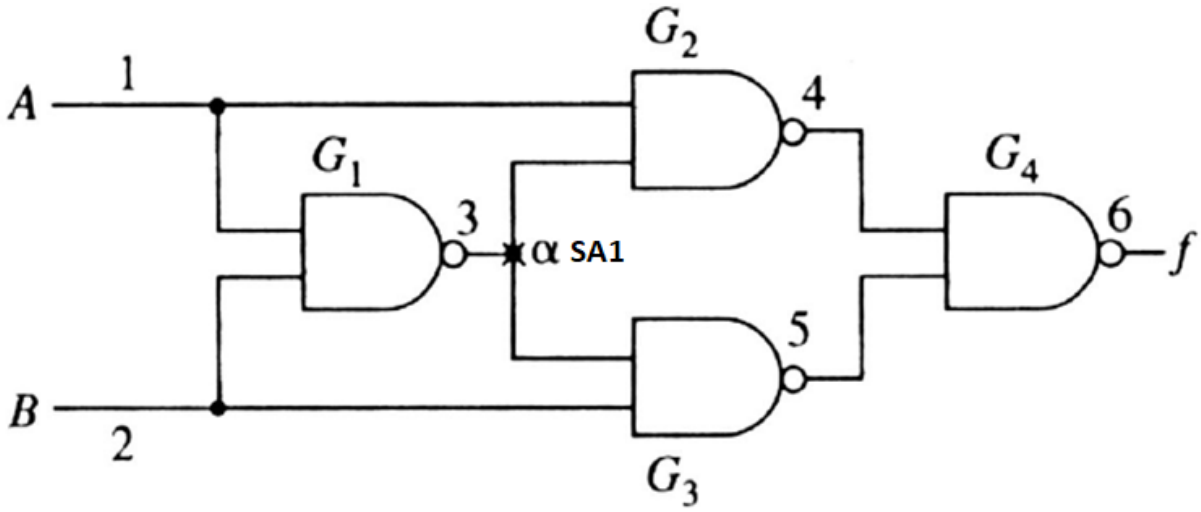

Figure 2B