Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FOURTH SEMESTER B.TECH. (E & C) DEGREE END SEMESTER EXAMINATION
APRIL/MAY 2019
SUBJECT: DIGITAL SYSTEM DESIGN USING VERILOG (ECE - 2204)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Implement an 8-to-1 multiplexer using an Altera MAX 7000 CPLD. Write the logic function and determine the number of macrocells required if parallel expanders are used.

1B. Realize the sequential circuit for the state table shown in **Table 1B** using ACT 2C and ACT 2S logic modules.

1C. Write switch level Verilog code of 3 input NOR gate using PMOS and NMOS switches.

(4+3+3)

2A. Write sequential Verilog code for one digit BCD counter and display the count value on seven segment display device. Assume common cathode configuration.

2B. (a) Find the controllability and observability at each line of the circuit in **Fig. 2B**.
(b) Draw the block diagram of ASIC design flow.

(5+5)

3A. Apply ITG to find the test vectors for the given circuit in **Fig 3A**.

3B. Write dataflow Verilog HDL code for 4-bit magnitude comparator.

3C. Explain various types of programmable interconnects used in Xilinx XC 3000 with neat diagram.

(4+3+3)

4A. Write the sequential Verilog code for negative edge triggered 4-bit binary-to-gray code converter with active high reset input.

4B. Implement the following functions using Xilinx XC 3000 FPGA. How many CLBs and LUTs are required? Show the contents of SRAM cell. (i) F1 = 3 variable majority gate (ii) F2 = 3 variable minority gate.

4C. Write a sequential Verilog code for 4-bit Ring counter.

(4+3+3)

5A. Write structural Verilog code for 4-bit adder/subtractor using full adder and 2-input XOR gate as basic building blocks.

5B. Write a structural Verilog code for Mod-8 asynchronous counter using T flip-flop as basic building block.

5C. Write a structural Verilog code for positive edge triggered D flip-flop as shown in **Fig. 5C**.

(4+3+3)

Table 1 B

		Y_1Y_2		z	
	y_1y_2	$x=0$	$x=1$	$x=0$	$x=1$
A	00	01	00	0	0
B	01	01	10	0	0
C	10	11	00	0	0
D	11	01	10	0	1

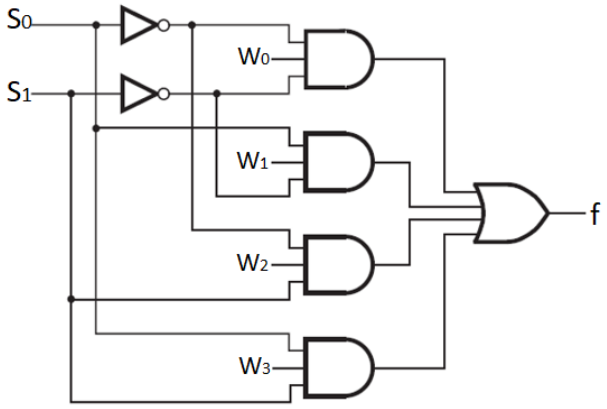

Fig. 2 B

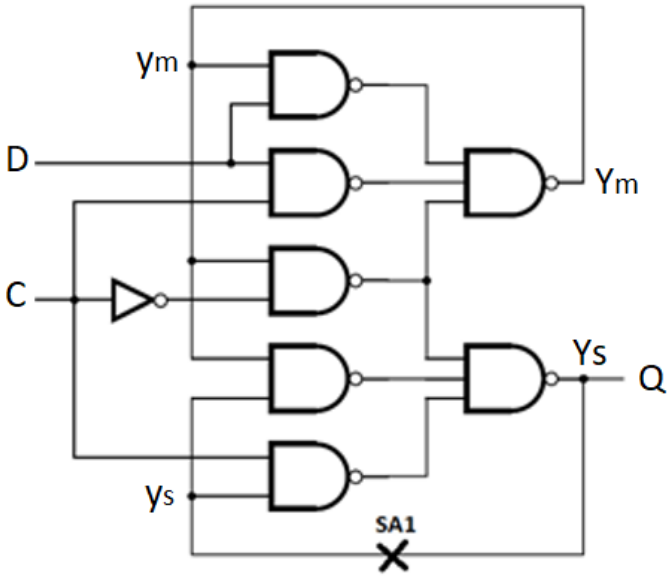

Fig. 3 A

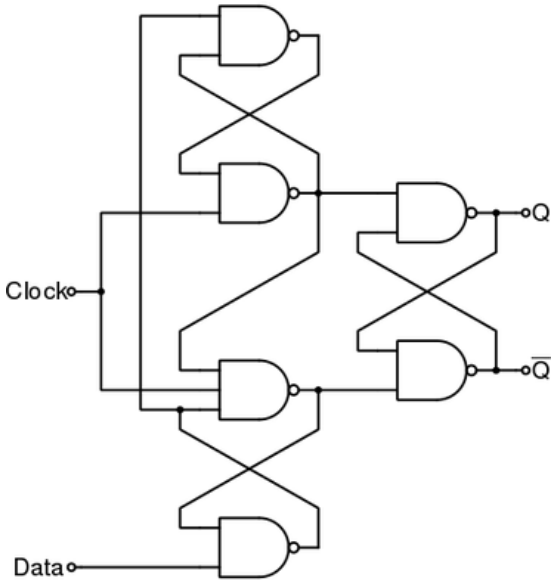

Fig. 5 C