Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FOURTH SEMESTER B.TECH. (E & C) DEGREE END SEMESTER EXAMINATION
APRIL/MAY 2019
SUBJECT: I C SYSTEMS (ECE - 2202)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Design a BJT based level shifter with the help of an active load to shift the DC level from 4V to 2V. Keep the power budget under 15mW.
Assume $\pm V_{CC} = \pm 6V$, $\beta = 100$, $V_A = \infty$, $I_S = 10^{-16}A$.

1B. For a dual input single ended differential amplifier, derive the expressions for differential gain and common mode voltage gain.

1C. An Op-amp is configured as inverting amplifier with a gain of 40 and -3dB bandwidth of 20kHz. The slew rate of the op-amp is 0.5V/μs. Determine the maximum peak to peak input signal that can be applied without distorting the output.

(4+3+3)

2A. Determine the input resistance of an inverting and non-inverting amplifier by assuming ideal op-amp. For the inverting amplifier shown in **Fig. 2A**, a) Determine the compensating resistor value to reduce the output offset voltage due to input bias current. b) Determine the maximum output offset voltage caused by the input offset current. Assume input offset current is 200nA.

2B. In the circuit shown in **Fig. 2B**, the op-amp is ideal. (i) Find V_N, V_P, and V_O (ii) Repeat part (i) if 40 kΩ resistor is connected in parallel with the 0.3mA source.

2C. Suggest the suitable circuit using an op-amp to deliver a current to a variable load resistor, one end of which is grounded. The current through the load is linear function of the source voltage and is independent of the load resistor. Derive the necessary expressions.

(4+3+3)

3A. Draw and design the op-amp based non-inverting Schmitt trigger circuit with UTP= +6V and LTP = +2V with the saturation voltage as ±10V and sketch the voltage transfer characteristics.

3B. Draw and design a 1kHz square wave generator using IC 555 for a duty cycle of 0.25. Assume C = 0.01μF.

3C. Discuss the operation of a FSK generator using 555 timer.

(4+3+3)

4A. With $C_1 = C_2 = C$ and $R_1 = R_2 = R_3 = R_4 = R$, obtain the transfer function for the circuit in **Fig. 4A** and show that it is an LPF.

4B. In the filter circuit shown in **Fig. 4B**, if $R_1C_1 = R_2C_2$, check if the circuit can act as a non-inverting integrator.

4C. For the gain plot in **Fig. 4C**, obtain the slopes at different intervals in i) dB/Decade and ii) dB/Octave

(4+3+3)

5A. Design a 4-bit binary weighted resistor type DAC whose full scale output voltage is -7.5V. Logic level 1 = +5 volts and logic level 0 = 0 volt. Determine the output when the input is (i) 0101 and (ii)1110. What is the resolution of the DAC designed? Select R = 10kΩ.

5B. Using 565 IC, design a circuit to get 20kHz clock from 2kHz clock and explain its working.

5C. Derive the 8-bit digital output equivalent to an analog voltage of 3V for an 8-bit dual slope ADC, which has a maximum integrator output of -8V when the input voltage is 12V.

(4+3+3)

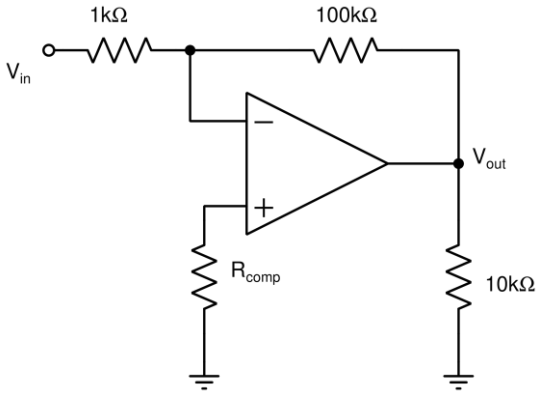

Fig. 2A

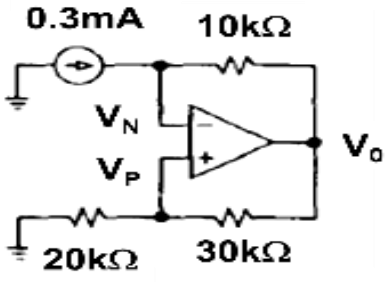

Fig. 2B

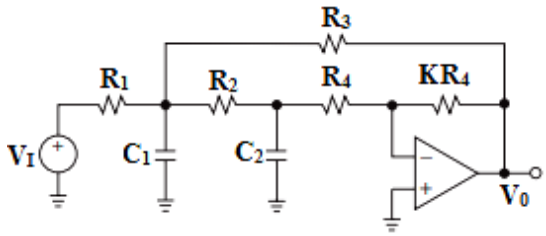

Fig. 4A

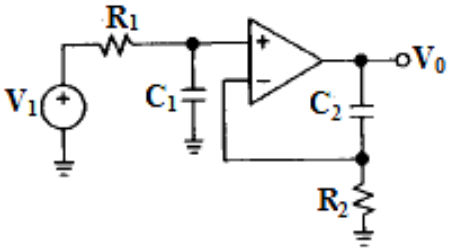

Fig. 4B

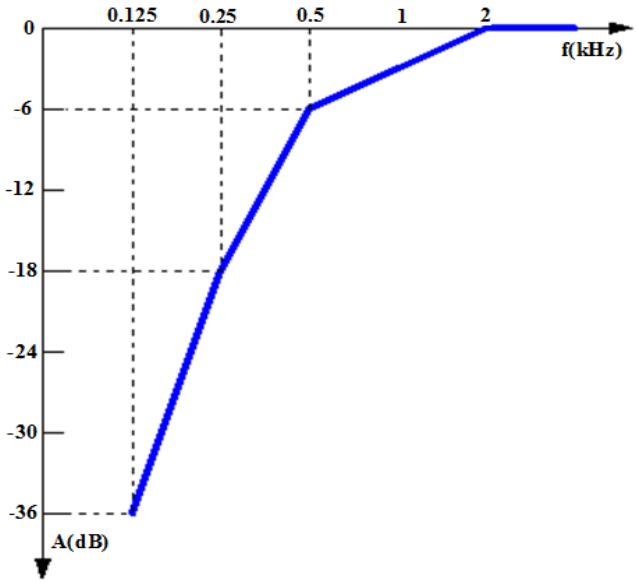

Fig. 4C